Improved coherence in optically defined niobium trilayer-junction qubits

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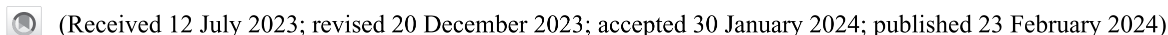

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Niobium offers the benefit of increased operating temperatures and frequencies for Josephson junctions, which are the core component of superconducting devices. However, existing niobium processes are limited by more complicated fabrication methods and higher losses than now-standard aluminum junctions. Combining recent trilayer fabrication advancements, methods to remove lossy dielectrics and modern superconducting qubit design, we revisit niobium trilayer junctions and fabricate all-niobium transmons using only optical lithography. We characterize devices in the microwave domain, measuring coherence times up to 62 μs and an average qubit quality factor above 10^5: much closer to state-of-the-art aluminum-junction devices. We find the higher superconducting gap energy also results in reduced quasiparticle sensitivity above 0.16 K, where aluminum-junction performance deteriorates. Our low-loss junction process is readily applied to standard optical-based foundry processes, opening alternative avenues for direct integration and scalability, and paves the way for higher-temperature and higher-frequency quantum devices.

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I. INTRODUCTION

A wide variety of superconducting devices have developed on the basis of Josephson junctions: their applications range from quantum-limited amplification and metrology [1–3] to digital logic [4–6] and they are an attractive platform for scalable quantum computing architectures due to their design flexibility and wide range of coupling strengths. Increasingly complex and robust quantum circuits have been demonstrated with aluminum junctions [7], however niobium is a tantalizing alternative superconductor due to its larger energy gap (and thus higher critical temperature and pair-breaking photon frequency) [8]. Taking advantage of this wider operating regime, niobium trilayer Josephson junctions became standard for single-flux-quantum circuits operating at liquid helium temperatures [4–6]. Employing these well-established fabrication processes, some early implementations of superconducting qubits were developed with niobium junctions [9–16]. However, these initial niobium qubits only retained quantum state coherence for less than 400 ns, diminished by coupling to sources of dephasing and dissipation in the junction and the qubit environment.

Minimizing these loss sources is crucial in all sensitive quantum systems, but particularly for qubits, which must remain coherent over the duration of many gate operations. Significant effort has since been dedicated to investigating and reducing sources of decoherence [17], demanding either adjustments of circuit geometry to limit or dilute coupling to spurious channels, or reducing the use of lossy amorphous dielectric materials. The need for insulated wiring contacts in these niobium trilayer junctions required growing passivating amorphous dielectric material in direct contact with the junction barrier, which likely degraded early qubit coherence [18,19], and limited their use in quantum devices. Higher temperature junctions with low loss promise a transformative source of strong nonlinearity for high-frequency quantum devices [20,21], and have since seen renewed interest from efforts to integrate digital and quantum logic [22–24], and the exploration of tunnel barrier materials beyond the limitations of aluminum [25–27]. Notably, by removing amorphous insulating scaffolding and increasing the circuit volume to reduce junction participation, qubits with epitaxially grown NbN junctions with crystalline AlN

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barriers have increased coherence times to 16 μs [28]. We apply similar improvements to traditional $Nb/Al/AlO_x$ processes, which are attractive due to the simpler deposition methods required.

In this paper, we revisit niobium trilayer junctions as the core component of transmon qubits and explore their coherence properties. We describe a method to form a temporary self-aligned sidewall-passivating spacer structure based on Ref. [29], which limits the amorphous spacer material to the smallest necessary region, and can later be chemically removed to further reduce dielectric loss. We find that high-temperature spacer-growth methods greatly reduce the critical current density of the junction barrier, allowing us to utilize exclusively optical lithography to fabricate high-nonlinearity junctions for microwave qubits. We find that our all-niobium qubits have lifetimes as high as 62 μs with an average qubit quality factor of 2.57×10^5: much closer to state-of-the-art qubits than past $Nb/Al/AlO_x$ devices [9–14]. We further observe that the higher superconducting gap energy results in reduced sensitivity to quasiparticles, particularly above 160 mK, where conventional aluminum-junction qubit performance deteriorates [30–32]. These results demonstrate the re-emergent relevance of niobium junctions for pushing the boundaries of superconducting devices.

II. TRILAYER FABRICATION

Despite niobium's attractive electrical properties, in thin layers its oxides are imperfect insulators with high dielectric loss [18,19], resulting in very poor natural tunnel junction barriers. Aluminum, on the other hand, forms a thin self-terminating oxide with low leakage and loss, but has a low critical temperature. The trilayer method leverages the strengths of both of these materials by using a thin layer of oxidized aluminum as the tunnel barrier and encapsulating it with niobium: through the proximity effect the Josephson junction inherits desired electrical properties and a clean tunnel barrier. This trilayer structure is typically grown on a wafer scale as the first step in fabrication, enabling excellent uniformity [33,34] and high purity-growth methods.

Our fabrication process (see Appendix A) is illustrated in Fig. 1. Similar to methods using sputtering, our trilayer is formed in a shadow-evaporation-compatible electron-beam system by depositing 80 nm of Nb and 8 nm of Al on high-purity single-crystal sapphire that has been annealed and chemically etched to remove surface damage. The deposition rate is kept high to maximize film quality (see Appendix B). To reduce defects and promote aluminum oxide formation [35], the aluminum is first ion milled then oxidized with an O_2-Ar mixture. To prevent oxygen diffusion into the Nb layer and the formation of lossy NbO_x [18,36], the oxidized Al surface is protected by a thin (3 nm) capping layer of Al. This layer is deposited while rotating the substrate at an angle for complete coverage while keeping it thin enough to avoid affecting junction properties. A (150-nm) thick counter electrode is then deposited on top, forming the trilayer *in situ*, without breaking vacuum.

The trilayer is patterned with *I*-line [37] photolithography and plasma etched in one step with Cl_2, BCl_3, and Ar to define the bottom electrode [Fig. 1(b)]. As it is necessary to make contact to the counter electrode without touching the base electrode, we then form an insulating sidewall-passivating spacer structure [29]. Amorphous

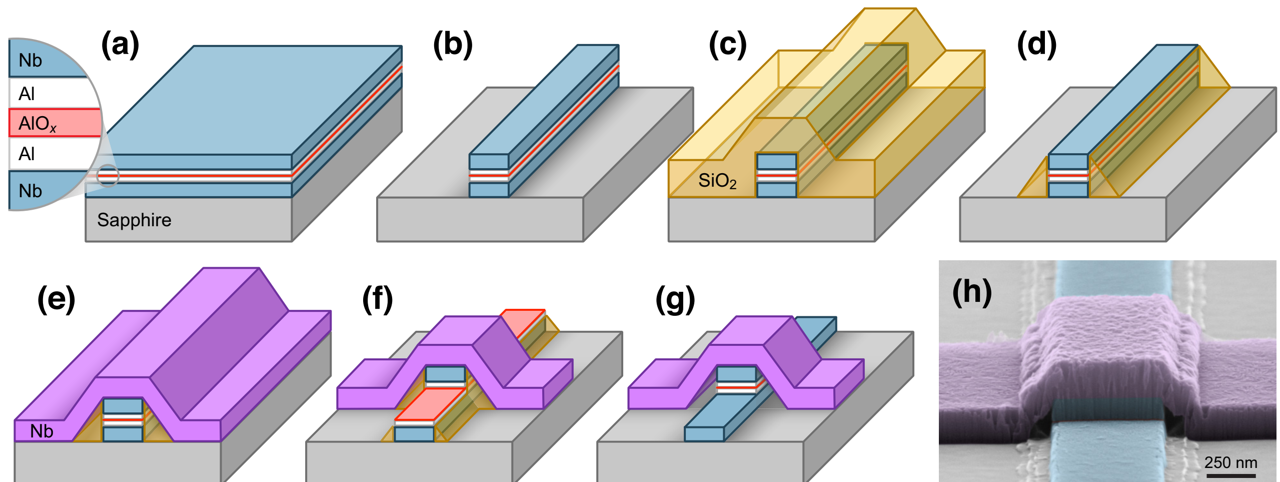

FIG. 1. Junction fabrication process. (a) Trilayer is deposited and oxidized *in situ*. (b) The first layer is etched with a chlorine RIE. (c) SiO_2 is grown isotropically. (d) Sidewall spacer is formed by anisotropic etching with fluorine chemistry. (e) Surface oxides are cleaned in vacuum and wiring layer (purple) is deposited. (f) Second junction finger (and other circuit elements) are defined by a fluorine plasma etch selective against Al. (g) Final devices undergo a wet etch to further remove SiO_2, exposed Al and some NbO_x. (h) Color-enhanced electron micrograph of a finished trilayer junction with dimensions 500 × 600 nm.

SiO_2 is grown isotropically [Fig. 1(c)] by either plasma-enhanced chemical vapor deposition (PECVD), which heats the wafer to 300°C for 16 min or high-density plasma-enhanced chemical vapor deposition (HDPCVD) (90°C). The SiO_2 is now etched anisotropically with a highly directional CF_4, CHF_3, and Ar plasma, which forms the spacer structure when the bulk material has been etched away [Fig. 1(d)]. The contaminated trilayer surface is ion milled, and the 160-nm Nb wiring layer is electron-beam-deposited on the sample [Fig. 1(e)]. We verify that this forms a low-resistance contact to the counter electrode (see Appendix B).

The wiring layer is patterned and a selective SF_6, CHF_3, O_2, and Ar plasma etch removes the wiring layer and the counter electrode, defining the perpendicular top junction electrode [Fig. 1(f)]. This etch is carefully optimized to minimize the formation of lossy fluorocarbon polymers [38] (see Appendix C) while preserving chemical selectivity: and although the plasma etches the Al layers far slower than Nb, the etch is still timed to finish a few seconds after the counter electrode is fully removed to limit excessive polymer deposition. Finally, to further remove the lossy amorphous materials present in the junction, a solution of NH_4F and acetic acid [39] are used to dissolve the remaining SiO_2: this process additionally removes any exposed Al and a small amount of surface NbO_x [Fig. 1(g)]. As this step can dissolve aluminum in the junction as well, etch times are kept below 15 s. This final treatment could likely be improved with a HF vapor etch, which has shown good results forming similar contact structures [40].

III. JUNCTION PROPERTIES

We verify the expected Josephson junction behavior [41] in our devices by measuring their hysteretic current-voltage curves in Fig. 2(a). When cooled to 860 mK, the unshunted junction shows a zero-resistance superconducting branch up to the critical current I_c, and an energy gap $2\Delta = 2.89$ meV. By comparing this value with critical temperature measured with resistivity, we find a relationship $2\Delta/k_BT_c = 3.61$: slightly lower than reported values for pure Nb [42,43]. Measuring the asymptotic normal-state resistance R_n above the energy gap we find a I_cR_n product of 1.5 mV, similar to values reported previously for Nb trilayer junctions [29,33,34,44,45]. Although measurements of the subgap region were limited by the experiment hardware, no excessive subgap leakage currents are observed.

Using the I_cR_n product found above, we can use room-temperature junction resistances to predict low-temperature properties [46,47]. Fitting the measured resistance for junctions of varying areas with two free parameters, specific resistivity and junction critical dimension bias (see Appendix D), we obtain the effective junction areas and the specific critical current density J_c for each wafer.

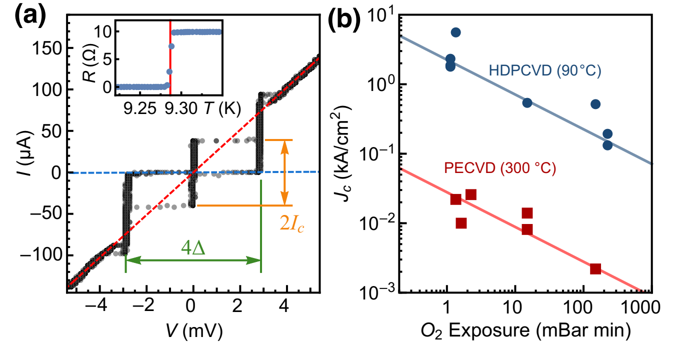

FIG. 2. Junction properties. (a) Current-voltage relations for an unshunted junction at 860 mK with $I_c = 38\ \mu A$ and an energy gap $2\Delta = 2.89$ meV. Bulk resistivity measurements (inset) give a critical temperature of $T_c = 9.28$ K. Above 4 mV, a linear fit (red dashed line) gives $R_n = 39\ \Omega$, and a fit to the subgap region (blue dashed line), estimates subgap resistance $R_s > 8\ k\Omega$. (b) Critical current density J_c (found by fitting room-temperature junction resistance as a function of junction area) as a function of oxygen exposure E measured for various wafers made with two deposition processes. The expected empirical $E^{-1/2}$ relationships are plotted as guides to the eye.

This method allows us to easily investigate effects of the fabrication process on junction electrical parameters. For Nb trilayers, the critical current density is sensitive to temperature [44] as well as oxygen exposure E, the product of oxygen partial pressure and oxidation time: this relationship has been empirically found to match $J_c \propto E^{-0.5}$ [29,44,48–50]. In Fig. 2(b) we plot J_c as a function of E for wafers with trilayers grown using various oxidation parameters and fabricated with two spacer deposition methods. For the HDPCVD junctions, we find critical current densities in the kA cm^{-2} range, comparable with other methods [29,44,45,51], and observe reasonable agreement with the oxygen exposure dependence described above. The effect of process temperature is readily apparent when we examine junctions with high-temperature-grown PECVD spacers: compared to HDPCVD junctions, we observe nearly a factor of 50 reduction in J_c. We find this temperature-annealing effect activates above 200°C (see Appendix E), in agreement with Ref. [44], and is likely the result of reduced barrier transparency [52] from diffusion.

IV. MICROWAVE QUBITS

With access to wide ranges of J_c, we can use PECVD-annealed junctions to realize qubit junctions with areas between 0.16–1.1 μm^2, which are large enough for optical lithography: while lower resolution than electron-beam lithography, this speeds up fabrication for devices with large numbers of junctions, and enables seamless integration with superconducting digital logic processes [6]. To investigate the junction performance in the context of quantum devices, we fabricate transmon qubits [53] in the

well-studied microwave regime (1–8 GHz). Aside from the junction we use a standard qubit geometry [54] (see Appendix F) capacitively coupled to a coplanar waveguide resonator for dispersive readout. The qubit capacitor, ground plane, and readout resonator are defined on either the base electrode or wiring layer, so no additional fabrication steps are needed. Chips with several qubits and their readout resonators sharing a common microwave feedline are characterized at the base stage of a dilution refrigerator (45–95 mK). Using microwave spectroscopy [53] we verify our qubits have anharmonicities around 140 MHz, and couple to their readout resonators with bare coupling strengths $g/h = 30$–60 MHz.

For superconducting qubits, the relaxation time and dephasing time are parameters of particular interest, as they dictate qubit limitations and act as sensitive probes for loss channels. We measure relaxation time by placing each qubit in its excited state and measuring it after time t: fitting the exponential decay gives the characteristic time T_1. We perform these measurements for each qubit and show averaged results as a function of qubit frequency in Fig. 3(a), finding $T_1 = 62.4$ μs for our best device. To probe loss channels in detail we use the frequency-independent qubit quality factor $Q_1 = \omega_q T_1$, which we find for our devices is on average above 10^5: within an order of magnitude of recent aluminum qubits [7,55–58] and similar to readout resonator quality factors (see Appendix G). We also perform a Ramsey experiment to measure the dephasing time T_2^*, and a Hahn-echo experiment to characterize the spin-echo dephasing time T_2. We find that T_2^* is within a factor of 2 of T_1, and particularly limited for lower-frequency qubits (particularly below 2 GHz), which experience increased environment noise, but also have increased charge sensitivity [53,59] leading to higher noise-dependent variation in qubit frequency. While this increases dephasing, these devices could be useful for investigating quasiparticle dynamics [59,60] in Nb. The T_2 values, which decouple slow frequency drifts are noticeably higher, demonstrated in particular by the charge-sensitive qubits from wafer B. This suggests that along with improved filtering, increasing the J_c for low-frequency qubits could improve dephasing by reducing charge dispersion [53].

Our qubits have relatively large junctions compared to typical designs [55–58] making them more sensitive to junction coherence properties. Using the energy participation ratio [55,61] of the junction $p_j = C_j/C_\Sigma$ in our devices, we can separate the loss contributions from the junction Q_j independent of other decoherence channels Q_0, expressing the qubit quality factor as a weighted sum $Q_1^{-1} = p_j/Q_j + p_0/Q_0$. We summarize qubit coherence properties with respect to their junction participation in Fig. 3(c). For our devices (red), we estimate an effective junction quality factor of 10^5: approximately 100 times greater than previous Nb/Al/AlO$_x$ qubits (blue) [9–16], and much closer to epitaxial NbN junctions (black) [26–28] and modern aluminum-junction qubits (green) [55–58]. Extrapolating to lower p_j values, we find our device loss is largely not limited by the junction, indicating that material refinements and device engineering could further improve qubit performance.

Compared to aluminum, niobium's higher gap energy leads to reduced device sensitivity to thermal quasiparticles [62], and shorter quasiparticle lifetimes [63], which

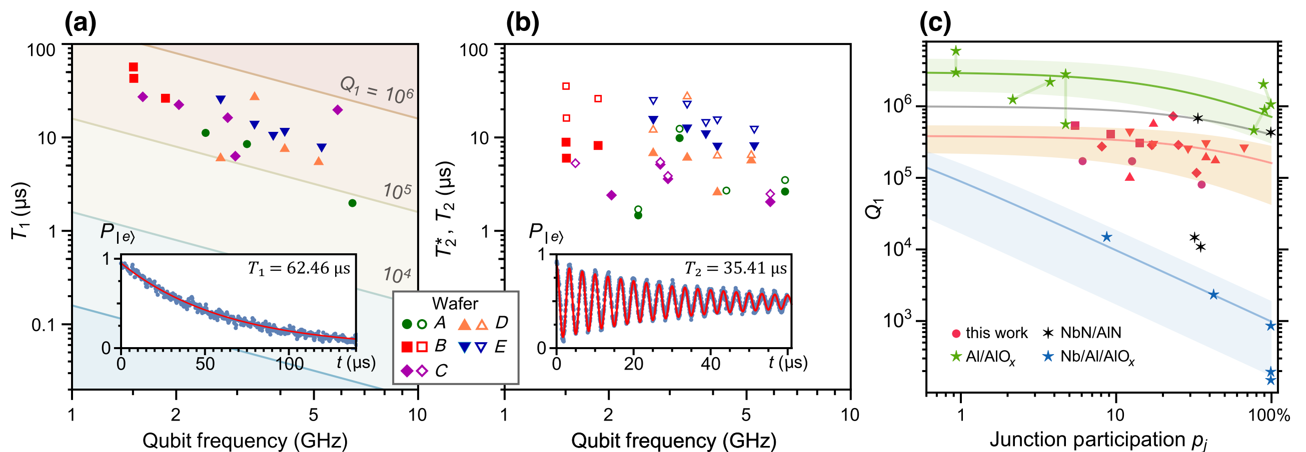

FIG. 3. Qubit properties. (a) Average qubit decay time T_1 extracted by fitting the exponential decay of excited-state population in (b) plotted as a function of qubit frequency, grouped by wafer. Lines indicate qubit quality factor $Q_1 = \omega_q T_1$. We find an overall mean Q_1 of 2.57×10^5 with some wafer-to-wafer variation. (c) Ramsey dephasing time T_2^* (filled points) and Hahn-echo dephasing time T_2 (hollow points) extracted by fitting the exponential decay of oscillations in (d) as a function of qubit frequency. We find an overall average T_2^* and T_2 of 6.643 and 12.916 μs, respectively. (e) Qubit quality factors as a function of their junction participation ratio plotted for devices in this work (reds) and in the literature (blue, black, green). Lines and shaded confidence regions show $Q_1^{-1} = p_j/Q_j + p_0/Q_0$ as a guide to the eye.

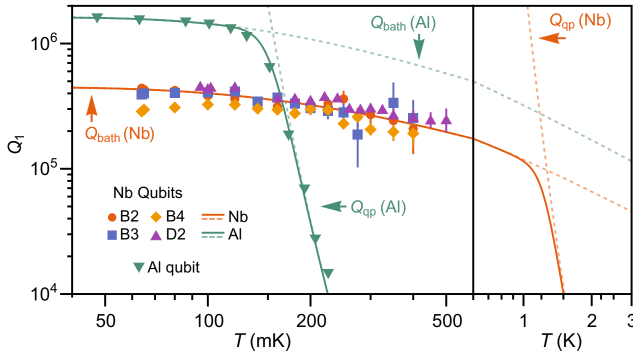

FIG. 4. Qubit quality factors from wafers B, D as a function of temperature. A mild decrease is observed at higher temperatures consistent with the system bath temperature Q_{bath}, however lifetimes are virtually unaffected by quasiparticles Q_{qp} (red lines). We also plot quality factors of an Al junction qubit, whose performance is noticeably limited by tunneling quasiparticles above 160 mK (green lines), whereas the Nb junction would not see an effect until about 1.1 K.

may help reduce the impact of nonequilibrium quasiparticles on qubit lifetimes [32,60,64,65]. To investigate this thermal resilience, we measure our qubits at increased operating temperatures, shown in Fig. 4. We observe a mild decrease in T_1 with temperature above 160 mK, consistent with heating from the environment bath [14], but importantly do not see the drastic temperature dependence expected for qubit loss induced by tunneling quasiparticles [60,65], in line with expectations for niobium. The advantage of higher-temperature junctions is apparent when comparing our qubit performance to an aluminum counterpart: above 160 mK, the aluminum qubit is quickly overwhelmed with quasiparticle-induced decoherence, whereas for our devices, T_1 is relatively unchanged. At such elevated temperatures, both devices face challenges from increased thermal microwave noise, motivating alternative qubit architectures [66,67] or higher qubit frequencies to explore this regime.

V. CONCLUSION

We have described a Nb/Al/AlO_x/Al/Nb trilayer fabrication method demonstrating a 100-fold improvement in junction loss at the single-photon level. By removing lossy dielectric materials wherever possible, we use our low current-density junction process to fabricate microwave transmon qubits using I-line photolithography demonstrating qubit quality factors within an order of magnitude of recent aluminum devices. Our qubits have relatively high junction participation ratios, which could either be reduced with smaller junctions (defined by electron-beam lithography) to improve coherence, or exploited further to significantly reduce qubit size [25,55].

Together with this device footprint flexibility, our all-optical qubit process opens the door to large-scale direct integration of scalable quantum processors with digital superconducting logic [22–24]. Niobium's higher energy gap significantly reduces sensitivity to quasiparticles for our junctions compared to aluminum analogues, allowing operation at much higher frequencies, and resulting in longer relaxation times above 160 mK where conventional qubit properties deteriorate. Combined with their low loss, which could be further reduced through material optimization [18,19,58], these properties make our trilayer junctions a promising candidate for quantum architectures with lower cooling power requirements, hybrid qubit systems requiring elevated temperatures, and enable alternative possibilities for nonlinear elements at millimeter-wave frequencies [20,21], paving the way for higher temperature, higher frequency quantum devices.

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APPENDIX A: FABRICATION METHODS

C-plane polished sapphire wafers are ultrasonically cleaned in toluene, acetone, methanol, isopropanol, and deionized (DI) water, then etched in a piranha solution kept at 40°C for 2 min and rinsed with deionized water. Immediately following, the wafers are loaded into a Plassys MEB550S electron-beam evaporation system, where they are baked by heating the stage to > 200°C under vacuum for an hour to help remove water and volatiles. When a sufficiently low pressure is reached ($< 5 \times 10^{-8}$ mbar), titanium is electron-beam evaporated to bring the load-lock pressure down even further. The trilayer is now deposited by first evaporating 80 nm of Nb at > 0.5 nm/s while rotating the substrate. After cooling for a few minutes, 8 nm of aluminum is deposited while rotating the substrate at

TABLE I. Plasma etch parameters used in the ICP-RIE etches described in the process. Etches are performed in an Apex SLR ICP etcher. Gas flows are listed in sccm.

	T(°C)	Pressure	ICP/bias power	Cl_2	BCl_3	Ar	CF_4	CHF_3	SF_6	O_2	Etch time	Etch rate
Etch 1 [Fig. 1(b)]	20 ± 0.1	5 mT	400 W / 50 W	30	30	10	–	–	–	–	50–60 s	~ 4.5 nm/s
Etch 2 [Fig. 1(d)]	20 ± 0.1	30 mT	500 W / 60 W	–	–	10	30	20	–	–	120–140 s s	~ 2 nm/s
Etch 3 [Fig. 1(f)]	20 ± 0.1	5 mT	400 W / 60 W	–	–	7	–	20	40	4	65–90 s	~ 4.5 nm/s

a shallow angle (10°) to improve conformality. The aluminum is lightly etched with a 400 V, 15 mA Ar^+ beam for 10 s, then oxidized with a mixture of 15% O_2:Ar at a static pressure between 2–50 mBar for 1.5–40 min. After pumping to below ($< 10^{-7}$ mbar), titanium is again used to bring the vacuum pressure down to the low 10^{-8} mbar range. We note that the pressure for the remainder of the trilayer deposition is higher than for the first Nb layer. The second 3-nm layer of Al is evaporated vertically while rotating the substrate to minimize void formation in the following layer. The counterelectrode is then formed by evaporating 150 nm of Nb at > 0.5 nm/s. The substrate is allowed to cool in vacuum for several minutes, and we attempt to form a thin protective coating of pure Nb_2O_5 by briefly oxidizing the top surface at 3 mbar for 30 s.

The wafers are mounted on a silicon handle wafer using AZ1518 photoresist cured at 115°C, then coated with 1 μm of AZ MiR 703 photoresist and exposed with a 375-nm laser in a Heidelberg MLA150 direct-write system. The assembly is hardened for etch resistance by a 1-min bake at 115°C then developed with AZ MIF 300, followed by a rinse in DI water. The entire trilayer structure is now etched in a chlorine inductively coupled plasma reactive-ion etcher (etch 1 in Table I). The plasma conditions are optimized to be in the ballistic ion regime, which gives high etch rates with minimal redeposition. Immediately after exposure to air, the wafer is quenched in DI water: this helps prevent excess lateral aluminum etching by quickly diluting any surface HCl (formed by adsorbed Cl reacting with water vapor in the air). The remaining photoresist is thoroughly dissolved in a mixture of 80°C n-methyl-2-pyrrolidone with a small addition of surfactants, which also removes the substrate from the handle wafer.

The wafer is ultrasonically cleaned with acetone and isopropanol, then SiO_2 spacer is grown by either HDPCVD or PECVD. For PECVD, SiH_4 and N_2O are reacted in a 100-W plasma with the chamber at 300°C. The complete process (including chamber-cleaning pumping and purging steps) takes approximately 15 min. For HDPCVD, the wafer is mounted on a silicon handle wafer using Crystalbond 509 adhesive softened at 135°C, then the spacer is deposited with a SiH_4 O_2 and Ar plasma, with the substrate heated to 90°C. The wafers are now etched in a fluorine reactive ion etch (etch 2 in Table I). This etch is optimized to be directional but in the diffusive regime to promote chemical selectivity while enabling the formation of the spacer structure. At this point minimizing oxide formation is crucial since the top surface of the trilayer is exposed and will need to form a good contact to the wiring layer, so immediately following the completion of the etch, wafers are separated from the handle wafer by heating to 135°C, ultrasonically cleaned of remaining adhesive in 40°C acetone and isopropanol, then immediately placed under vacuum in the deposition chamber, where they are gently heated to 50°C for 30 min to remove remaining volatiles.

The contaminated and oxidized top surface of the counter electrode is etched with a 400 V, 15 mA Ar^+ beam for 5 min, which is sufficient to remove any residual resistance from the contact. After pumping to below ($< 10^{-7}$ mbar), titanium is used to bring the vacuum pressure down to the low 10^{-8} mbar range. The wiring layer is now formed by evaporating 160 nm of Nb at > 0.5 nm/s. The substrate is allowed to cool in vacuum for several minutes, and the wiring layer is briefly oxidized with 15% O_2:Ar at 3 mbar for 30 s to promote a thin protective coating of pure Nb_2O_5. The wafers are again mounted on a handle wafer, coated with AZ MiR 703 photoresist and exposed with a 375-nm laser. The assembly is hardened for etch resistance by a 1-min bake at 115°C before development. The final structure is now defined with a fluorine reactive ion etch (etch 3 in Table I). This step proves to be highly problematic as it easily forms inert residues, and needs to be highly chemically selective in order to avoid etching through the aluminum, so the plasma is operated in a low-density ballistic regime with the addition of O_2, which helps passivate exposed aluminum and increase selectivity. The etch time is calculated for each wafer based on visual confirmation when the bare wiring layer is etched through. We remove cross-linked polymers from the photoresist surface with a mild 180-W room-temperature oxygen plasma that minimally oxidizes the exposed Nb (though find this is not very effective). The remaining resist is now fully dissolved in 80°C n-methyl-2-pyrrolidone with surfactants.

With the junctions now formed, the wafer is ultrasonically cleaned with acetone and isopropanol, coated with a thick protective covering of photoresist (MiR 703) cured at 115°C, and diced into 7-mm chips. The protective covering is now dissolved in 80°C n-methyl-2-pyrrolidone with surfactants (we find this can also help remove stubborn organic residues from previous steps), and the chips are given a final ultrasonic clean with acetone and

isopropanol. The remaining silicon spacer is now dissolved by a short 10–15 s etch in a mixture of ammonium fluoride and acetic acid (AlPAD Etch 639), quenched in deionized water, then carefully dried from isopropanol to preserve the now partially suspended wiring layer. The finished chips are packaged and cooled down within a couple hours from this final etch to minimize any NbO_x regrowth from air exposure.

APPENDIX B: JUNCTION SUPERCONDUCTOR PROPERTIES

Josephson junction properties are largely determined by the characteristics of the two superconductors and the insulating oxide barrier that separates them, so the initial formation of the trilayer materials is crucial for the device quality. As niobium sets the limit of superconducting properties and losses in our junctions and qubits, it is crucial to begin with a high-quality and thus high-purity material. Maintaining material purity presents a challenge for any thin-film deposition technique, made difficult in particular by the incorporation of contaminants into the film during growth. This contamination can be addressed with two main approaches: first by reducing the flux of contaminants (achieved by reducing the vacuum pressure during the deposition process), but also by reducing the duration of exposure, which can be controlled by the deposition rate.

For electron-beam evaporation (the deposition technique used here) vacuum pressures are reduced as low as possible during deposition, however are limited to the 10^{-8} mbar range by the hardware. With the contaminant flux fixed by the deposition system vacuum pressure, we explore the effect of deposition rate on Nb purity. By measuring the resistivity of a film with a known geometry at varying temperatures, we obtain a wealth of information about the film properties. In Fig. 5(a) we plot the superconducting transition temperature T_C (proportional to the superconducting gap Δ_0) as a function of metal deposition rate. We observe that higher rates yield increased transition temperatures, which approach those found in bulk high-purity Nb [68], indicating that the films are increasingly pure. Indeed, we can also correlate the residual resistivity ratio RRR $= \rho(300\text{ K})/\rho(T_C)$, an indicator of superconductor quality, with deviations of measured critical temperature the bulk value T_C^{bulk}, supporting the notion that higher deposition rates yield higher-quality films. Due to the extreme local temperatures required, practical considerations and stability concerns put a limit on feasible deposition rates. Nonetheless, despite variations induced by vacuum conditions, we find that rates above 0.6 nm/s are required to deposit a film with high purity.

We can go further to examine the degree of disorder in the superconductor by probing the kinetic sheet inductance $L_K = \hbar R_\square/\pi\Delta_0$ where $R_\square = \rho_0/t$ is extracted from the film thickness t, and the resistivity just above the superconducting transition. The sheet inductance also yields the London magnetic penetration depth $\lambda_L^2 = tL_K/\mu_0$. In Fig. 5(b) we find that both L_K and λ_L are also reduced with films deposited at higher rates. Lower kinetic inductance and shorter London lengths indicate a lower degree of disorder in the superconductor, suggesting that increased deposition rates bring the material further away from the disordered dirty superconductor limit ($\lambda_L \gg \xi$) [69].

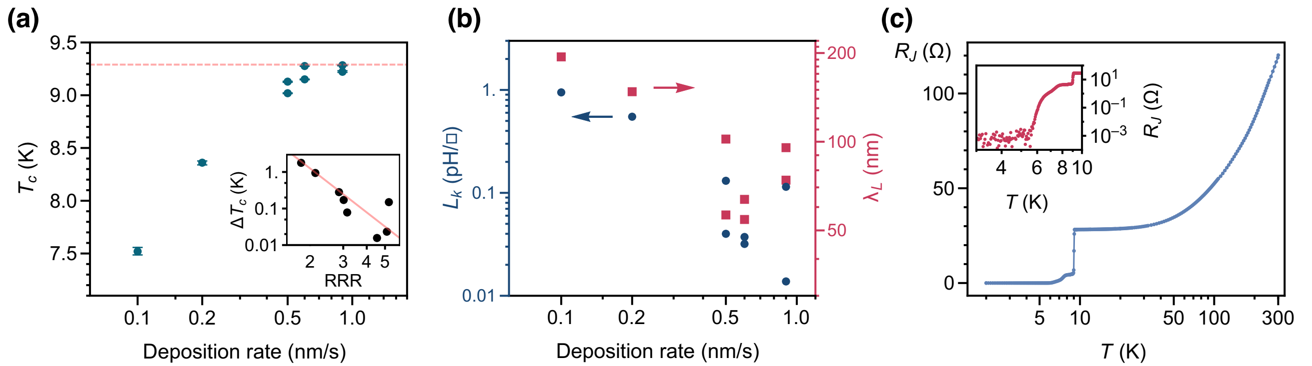

FIG. 5. Superconductor material quality. (a) Niobium superconducting critical temperature T_C extracted from resistivity measurements as a function of metal deposition rate. At rates above 0.6 nm/s, T_C approaches bulk value (dashed line). The inset shows deviations from bulk $\Delta T_C = T_C^{\text{bulk}} - T_C$ are correlated with the residual resistivity ratio, implying high deposition rates result in high-quality films. (b) Sheet kinetic inductance L_k and observed London penetration depth λ_L plotted as a function of deposition rate suggesting that films deposited at higher rates are closer to the clean superconductor limit. (c) Specific junction resistance $R_J = R/N$ obtained by measuring the resistance R of a chain of $N = 12$ junctions as a function of temperature. A sharp drop in resistance is observed above 9 K as the niobium electrodes begin to superconduct. As the temperature decreases, the junction critical currents increase above the excitation current (10 μA), and below 5 K the measured resistance drops to zero as the excitation is confined to the superconducting branch, indicating proximitization of the aluminum and superconducting contact between the counterelectrode and wiring layers.

We verify the superconducting contact quality between the wiring layer and the counterelectrode, as well as the junction tunnel barrier transparency by measuring the voltage accross a chain of 12 junctions in series, through which we send a fixed excitation current of 10 μA. In Fig. 5(c) we plot the per-junction specific resistance R_J as a function of temperature, showing the immediately apparent superconducting transition above 9 K. Immediately below the transition, the superconducting gap is still relatively low, and the junction critical currents fall below the excitation current, so a small resistance is observed. However, as we decrease the temperature, we find that the resistance shrinks by several orders of magnitude (below the noise floor of the instrument). This indicates that the sum of any remaining resistance channels in a single junction is likely well below the mΩ range, suggesting a superconducting contact between the Nb wiring layer and the Nb counterelectrode.

In a superconductor the residual resistivity ratio is also correlated with grain size in the film [58,70,71]. For a junction wiring layer deposited at 0.9 nm/s we observe a RRR of 4.45, indicating good quality relative to the films we produce [see Fig. 5(a)]. From the scanning-electron-microscope image shown in Fig. 6(a) we observe a short-range ordered microscopic grain structure in the regions where the wiring layer is deposited directly on the exposed sapphire substrate. A high-resolution top-down SEM image shown in Fig. 6(b) reveals a network of thin grains with a visible hexagonal arrangement. Interestingly, since the crystal structure within niobium grains is expected to be cubic [70] this suggests the long-range hexagonal order is a reflection of the *C*-plane sapphire substrate surface. The individual grains (distinctly larger than the 1–4 nm grains of the Pt and Pd film used to reduce charging in the image) are significantly elongated in one dimension. To get a sense of the grain size, we measure the short dimension of a grain [as shown in Fig. 6(b)] for a number of grains visible in the image, and summarize the results in Fig. 6(c). By fitting to a normal distribution, we find an average grain width of 16.386 nm, with some skew towards longer widths. Notably we do not see the expected T_c reduction from this grain size [70,71] since we find the measured T_c for this film is relatively close to the bulk value [8,68]. This suggests that the shortest dimension of the grains does not limit superconductor performance. We can instead extract an average grain area of $d \times l \simeq 1638$ nm^2 for our film, which corresponds to an effective grain size of $d_{\text{eff}} = \sqrt{ld} \simeq 40.47$ nm, from which we expect properties similar to bulk [70,71]. Further investigation using x-ray diffraction or transmission electron microscopy [18,58,71] could reveal even more details about the microscopic properties of the niobium.

APPENDIX C: LOSSY PLASMA-ETCH RESIDUES

By virtue of size, the electric field concentration in a junction is orders of magnitude higher than in the qubit capacitor (or any planar structure such as the resonator capacitor), meaning the participation ratio [61] of the junction side surfaces will also be much higher. As such, our junction loss is likely still limited by the presence of lossy dielectrics formed on the sides of the junction, which for our design are primarily either spacer material, metal oxides, or residues left by the reactive ion-etching process. As we cannot use more aggressive spacer [40] or oxide removal methods [18] without further risking the integrity of the aluminum junction barrier, we instead study the etch residues and discuss mitigation strategies.

Alongside the desired chemical and mechanical processes that remove niobium, reactive ion etching hosts a variety of simultaneous mechanisms that can grow

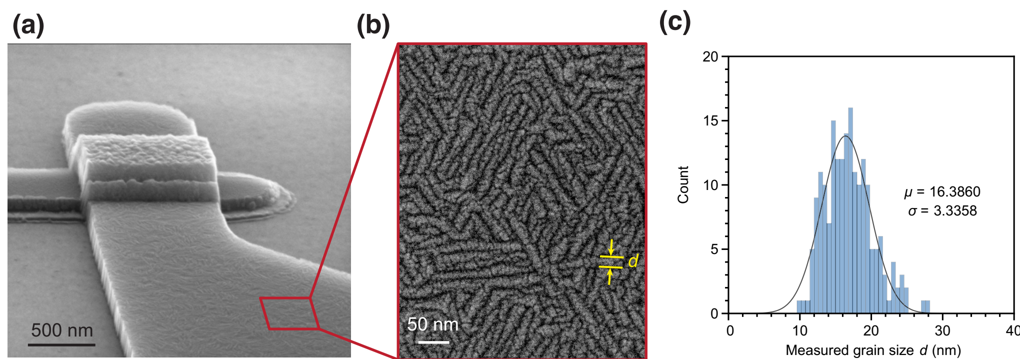

FIG. 6. Superconductor grain size. (a) In a tilted scanning-electron-microscope image of a junction, microscopic grains are observed on the metal surface. In regions of the wiring layer that lie directly on the sapphire substrate, the columnar grain growth is uninterrupted, and the grain pattern is transferred to the top surface of the metal. (b) A top-down high-resolution scanning electron micrograph reveals the hexagonal arrangement of the grains. The grain size can be estimated by measuring the narrow dimension of a grain, marked *d*. (c) A histogram of repeated measurements of grain width are fitted to a normal distribution, which suggests an average grain width of 16.386 nm.

material: etched material can either be redeposited by sputtering, low-energy reaction products can readsorb onto exposed surfaces, and components in the plasma can react with exposed material [38]. The products of all of these mechanisms tend to be much more difficult to remove, so end up staying behind after the photoresist is dissolved, particularly on vertical walls not directly exposed to plasma bombardment during the etch. While the deposited material passivates the walls of the etched region during the etch and can produce high-aspect ratio features, for our junctions its critical to reduce any excess dielectrics, so we explore ways to understand and mitigate these residues in order to reduce loss.

In Fig. 7(a) we show an example of a dielectric residue located on the side of a junction, which has not been removed throughout the entire fabrication process. This material must be formed during the third dry etch [Fig. 1(f)] since it covers and extends off the sides of the Nb wiring and counterelectrode layers. The residues appear to be present on all vertical surfaces exposed by the etch, visible as striations on the junction sides. To determine the deposition mechanism for this residue, we probe the chemical composition of the residue using energy dispersive spectroscopy (EDS). A composite map of normalized element composition is overlaid on the same image of the residue in Fig. 7(b), with individual normalized element concentration maps shown to the right. As expected, we observe high Nb concentrations in the metal regions, and high aluminum and oxygen concentrations in the sapphire region, but what is more we observe a significant concentration of fluorine in the residue (carbon is also observed in this region as well, but cannot be quantified due to high background carbon levels). This heavily suggests the residue is some kind of fluorocarbon polymer.

Fluorocarbons are chemically inert and robust against most standard solvents, acids, or oxygen plasma, and the residues remain largely unaffected by these conditions. However, fluorocarbon polymers are susceptible to defluorination by strong alkali reductants such as sodium-potassium amalgam (NaK) [72,73]. In Fig. 8(a) we show a device with particularly extensive residues covering and extending off the sides of the wiring layer. In an oxygen-free dry nitrogen glovebox, we immerse the sample surface in a sodium-potassium amalgam (NaK) for 15 min, rinse with tetrahydrofuran, move the sample into air, finish rinsing with acetone and isopropanol, then image the residues. In Figs. 8(b) and 8(c) we observe that the residue material is largely removed: the overhanging features have been removed, as well as the material on metal sides, with the original extent of the residue (about 30 nm) apparent by the indentation left on the sapphire by the residue during the etch. This corroborates the hypothesis that these residues are composed of fluorocarbons, since the material could be removed upon treatment with NaK, wherein the amalgam cleaves the problematic C—F bonds and allows the remaining residues to become soluble in organic solvents.

While this NaK treatment appears promising on the microscopic scale, in practice the amalgam is difficult to keep clean, and leaves behind significant quantities of dust and salt deposits on the chip surface. A more practical method to postclean any residues left behind by the etch might be to instead use a solution with a high reducing potential such as sodium napthalenide [72], commonly used as a surface treatment for PTFE. Regardless, the best way to remove the residues is to not form them in the first place, which is achieved by optimizing the etch plasma conditions. First, we remove obvious residue sources by ensuring the plasma chamber is thoroughly cleaned with oxygen, and no fluorinated vacuum oils are present in the system. We find that using gas constituents with low hydrogen and carbon content (e.g., SF_6 or CF_4) significantly reduces the residue growth: in particular we find CHF_3 and C_4F_8 readily polymerize. However, we note that using too much SF_6 can lead to the incorporation of sulfur [74] into any exposed SiO_2, which forms an even

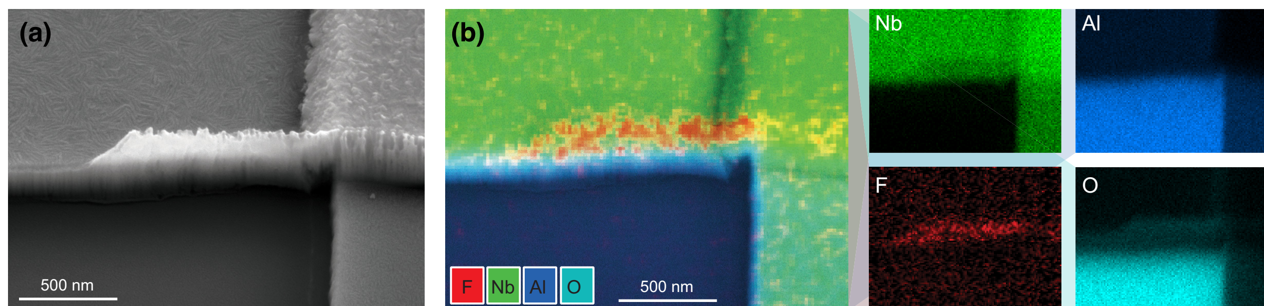

FIG. 7. Etch residue chemical analysis. (a) Scanning electron micrograph of a plasma etch residue located on the wiring layer near a junction. (b) Composite energy dispersive spectroscopy (EDS) image overlaid on the image in (a) showing normalized element density regions for F, Nb, Al, and O, with individual element density maps shown in their respective color on the right. Along with clear Nb and sapphire (Al_2O_3) regions, a high concentration of fluorine relative to the background is found in the residue region, suggesting the residue is composed of fluorinated polymers.

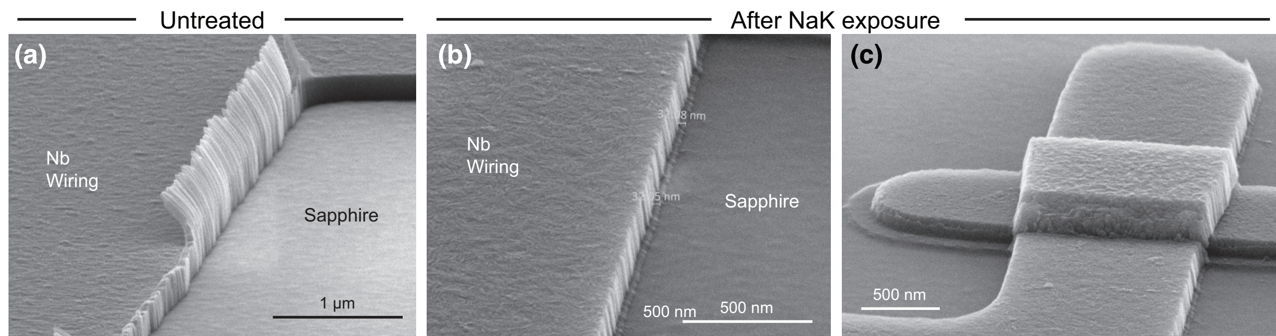

FIG. 8. Etch residue NaK reactivity. (a) Scanning electron micrograph of a plasma etch residue on the edges of the wiring layer. A closer inspection of the bottom left reveals that the residue extends to cover the sides of the metal, even where the top crust has been mechanically removed. (b),(c) The wiring layer and a junction from the same wafer imaged after a 15-min exposure to sodium-potassium amalgam (NaK) showing nearly complete removal of the etch residue.

more inert residue and should be avoided. The addition of O_2 in the plasma can also help increase the carbon-fluorine ratio of the plasma [75], but also increases resist etch rate [76] and may passivate exposed metal [77], which affects the etch profile. Using a low-density plasma with a long mean free path for the radicals is key to increasing the etch rate and reducing redeposition, as it increases the effective reactant and product temperature. Residue formation is also particularly sensitive to substrate temperature. With the substrate too cold, the reaction product temperature becomes low enough to allow recondensing, leading to increased fluorocarbon deposition. If the substrate is too hot, reactivity of the photoresist polymers is increased, promoting crosslinking, polymerization, and fluorination: thus good thermal contact between the substrate and the carrier wafer is essential, as the high-temperature plasma can otherwise significantly heat the substrate. Finally, we observe the residue formation accelerates when the insulating substrate is exposed (likely a result of screening charges focusing the plasma towards remaining metal), so we ensure the etch is stopped within 15 s of completion.

APPENDIX D: JUNCTION AREA DEPENDENCE, VARIATION, AND STABILITY

Having verified the relationship between the normal-state resistance R_n, the critical current, and the gap energy [47] (see Fig. 2), we can use room-temperature resistance measurements to efficiently predict cryogenic junction properties. In Fig. 9(a), we show room-temperature junction resistance and junction inductance (calculated from resistance using the I_cR_N product), plotted as a function of junction area (corrected for lithographic reduction). The original untreated [see Fig. 1(f)] junction resistances are in good agreement with the expected inverse dependence on junction area, enabling us to fit the original critical current density. After etching the spacer [see Fig. 1(g)] some of the aluminum is removed as well, and the resistance increases since the effective junction dimensions have shrunk. By fitting the etched junctions, we extract a dimension reduction of approximately 160 nm, which corresponds to about 80 nm of aluminum that gets removed by the etch. We note that this sets a practical limit on how small the junction can be before etch effects become more significant than lithographic definition of junction area.

Fitting junction resistances as a function of the final junction area (taking into account the dimension reductions) yields the true critical current density for the final junctions [Fig. 9(b)]. We repeat these measurements for wafers with different processing conditions to populate Fig. 2(b). A spread (typically between 5–10%) is noticeable in our junction resistance for a given junction area. While higher than typical niobium trilayer junction nonuniformity [33,34], our junction variance can primarily be attributed to relatively large geometric deviations due to the limits of our lithographic resolution, which is compounded by fluctuations in the etch dynamics that determine the final junction area. This implies that our junction parameter spread could likely be reduced with higher-resolution lithography methods and a more selective spacer removal technique. We test the functional limits of our junction reproducibility by measuring deviations of qubit frequencies across different chips from different wafers. In Fig. 9(c), we show spectroscopically measured qubit frequencies (determined by junction inductance) as a function of design qubit junction area for devices with two different qubit capacitor designs. After determining the qubit capacitance and applying the estimated junction area reductions, we find the measured frequencies are self-consistent within 10% or so, even across separate wafers.

We can investigate the variation of junction properties in more detail by repeating the measurements in Fig. 9(b) for chips in different physical locations across a 2-inch diameter wafer. We plot the results by their original position in the wafer and summarize the results in Fig. 10(a).

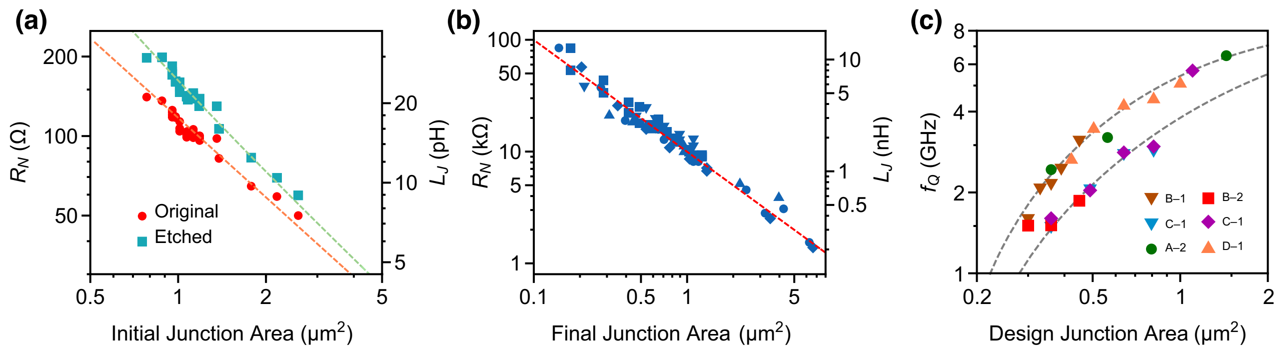

FIG. 9. (a) Room-temperature junction resistance and junction inductance plotted as a function of junction area (corrected for lithographic reduction). Original untreated junction resistances are shown in red, and etched junctions in teal, with fits to an inverse relationship to area (dashed lines) yielding the original critical current density J_c and an etch dimension reduction of approximately 160 nm. (b) Junction resistances as a function of the final junction area with a inverse fit (dashed line), which gives the critical current density. For illustrative purposes we have shown PECVD junctions in (a) and HDPCVD junctions in (b). (c) To estimate reproducibility, spectroscopically measured qubit frequencies are plotted as a function of design junction area, labeled by wafer and cooldown. Expected values for the two different qubit capacitor designs (120 and 160 fF) are shown with dashed lines.

We find that the fitted critical current density fluctuates from chip to chip, consistent with the typical 5–10% junction variation observed in Fig. 9(b). Additionally, we observe a wafer-scale radial dependence in extracted critical current density, with noticeably lower values near the edge of the wafer. This is likely caused by a combination of dimension deviations from optical lithography and RIE etch rates, both of which have a wafer-scale radial dependence in our process. To estimate this lithographic dimension variation, we examine the statistics of measured junction area within a single chip relative to the expected area (with critical dimension bias taken into account), summarized in Fig. 10(b). Notably the measured areas are distributed with a standard deviation of 13.53% relative to the expected area: when accounting for the 5% accuracy of the area measurement, the remaining spread accounts for a significant amount of the fluctuations observed in junction parameters. Thus we estimate that the dominant source of junction parameter variation is a result of dimension variation from optical lithography along with further dimension variation from fluctuation in etch dynamics. Process uniformity and lithographic dimension conformity are extensively studied topics [33,34,44], so we believe that applying these techniques or moving to higher-resolution lithography (stepper or electron beam) [28,34] could help decrease junction parameter variation.

Josephson junctions are known to change with age [44,78], so it is also worthwhile to investigate the long-term stability of junction parameters, particularly for our design, which leaves the junction barrier exposed from the side. To this end, we remeasure junctions after 5 months of storage in air. In Fig. 10(c) we show the relative change in

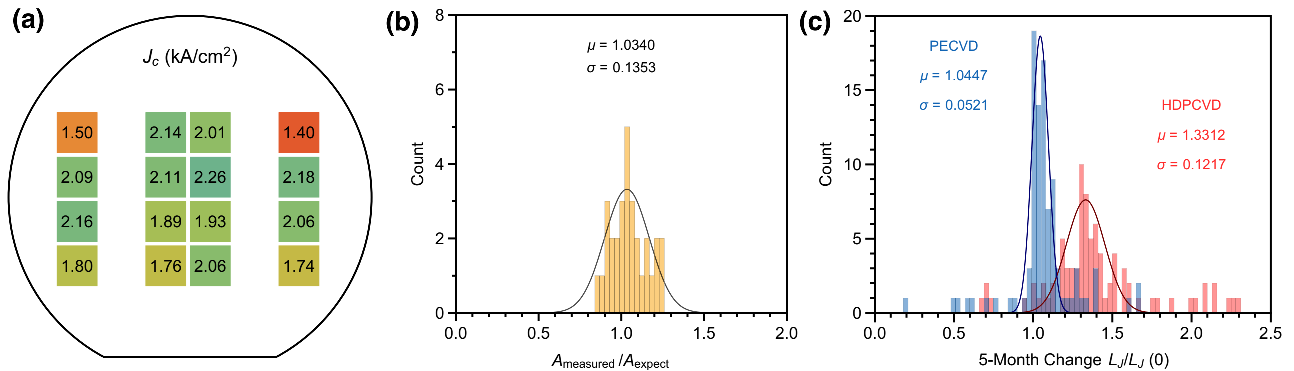

FIG. 10. (a) Average junction critical current density on an individual chip measured across several chips across a 2-inch wafer, with deviations from nominal values (2.088 kA/cm^2) highlighted with color. (b) Junction area measured with optical microscopy relative to the expected design area, highlighting the distribution of deviations resulting from lithography. (c) Long-term stability of junctions measured by the relative change in Josephson inductance for 5-month-old junctions relative to their original values. Notably the change in high-temperature PECVD junctions is much lower than HDPCVD junctions.

calculated junction inductance for both high-J_c HDPCVD junctions as well as low-J_c PECVD junctions after the storage period. In both cases we observe an expected increase in J_c from diffusion in the junction barrier with age [44,78]. The aged high-temperature PECVD junctions show a mean J_c increase of about 4.5%, significantly lower than the low-temperature HDPCVD junctions, which exhibit a critical current-density increase around 33% along with a wider distribution. This suggests that for the high-temperature PECVD junctions, the aging mechanism in the junction barriers is accelerated during the fabrication process.

APPENDIX E: JUNCTION ANNEALING MECHANISM

The effect of process temperature is readily apparent when comparing the resulting critical current densities of junctions with PECVD spacers (deposited at 300°C) and those with HDPCVD-grown spacers (90°C). In Fig. 2(b), for the high-temperature PECVD junctions, we observed an approximately 97.7% reduction in J_c. We investigate this effect in more detail by annealing finished low-temperature (HDPCVD) junctions with initial $J_{c0} \sim 3$ kA cm^{-2} in a dry Ar atmosphere, then remeasuring their critical current density.

In Fig. 11(a), we plot the annealed J_c as a percentage of the untreated J_{c0}, and confirm that the annealing effect activates above 200°C, in agreement with Ref. [44]. In Fig. 11(b) we show the critical current density of junctions annealed at 300°C for various lengths of time. After about 20 min (the approximate time wafers spend at 300°C during PECVD) we find that the current-density reduction approaches the measured ratio between the PECVD and HDPCVD junctions. This suggests the high-temperature process dynamically anneals the junction barrier, likely increasing mobility in the oxide barrier, which enables diffusion and reduces pinhole density [52]. Qualitatively, this process appears to be exponential in time, so we overlay a saturating exponential fit of the form $J_c/J_c^0 = (1-\alpha)e^{-t/\tau} + \alpha$, where α is the observed reduction factor, and obtain a critical time $\tau \approx 4$ min. The observed annealing effect is consistent with the critical current densities measured in Ref. [29], which do not exceed 190°C during the fabrication process. With this in mind, our PECVD process could be modified to produce high critical current-density junctions by either reducing the deposition temperature below 200°C or to a lesser extent by limiting the time spent at elevated temperatures. This would allow for improved process stability by providing control over a wide range of critical current densities in a unified process, eliminating the need for switching between PECVD and HDPCVD deposition methods.

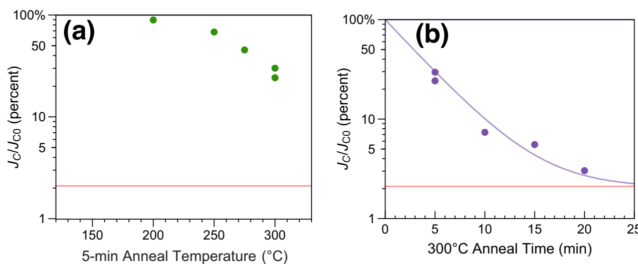

FIG. 11. (a) HDPCVD junction critical current-density reduction after annealing for 5 min plotted as a function of anneal temperature showing activation at 250°C. (b) Critical current-density reduction as a function of anneal time at 300°C, which approaches the factor of 50 reduction observed in the main text (red lines). The purple line represents an exponential fit saturating at the observed reduction factor.

APPENDIX F: QUBIT GEOMETRY AND EXPERIMENTAL SETUP

The qubit, readout resonator, and other structures are formed in the same steps as the junction. We base our design on a qubit geometry [54] popular for its reduced radiation profile, a result of the cross-shaped coplanar qubit capacitor whose local electric dipole moments act to cancel each other out far away. In our case, the cross shape (typically used to implement qubit-qubit coupling or additional charge drives) is not strictly necessary and a coplanar capacitor composed of any two-dimensional shape would work as well. We also make an effort to minimize coupling to lossy two-level systems in surface dielectrics by rounding sharp corners where possible in the geometry. This reduces electric field concentration at specific points in the capacitor, leaving a weaker and more homogenous electric field, which should couple less strongly to individual two-level systems.

An example of our qubit geometry is shown in a composite microscope image on the top right of Fig. 12, imaged after etch 3 [Fig. 1(f)]. The niobium and unetched aluminum have visibly different colors, allowing us to distinguish between the wiring layer and the base electrode. In our geometry, the qubit capacitor is formed with both layers, while the rest of the circuit and the majority of the chip (ground plane, readout resonator, and coupling waveguides) is formed with just one layer. We find that the wiring layer readout resonators exhibit lower loss (see Appendix G), so typically pick the wiring layer for the ground plane. However, having measured devices with both configurations (majority wiring layer and majority base electrode), we do not find extreme differences in qubit properties, where the fields participate in both layers regardless of orientation. As an example, compare base-electrode ground plane wafer *D* with wiring ground plane wafer *A* in Fig. 13(b), whose quality factors are similar.

The qubits are capacitvely coupled to a meandered quarter-wave coplanar waveguide resonator, which is in

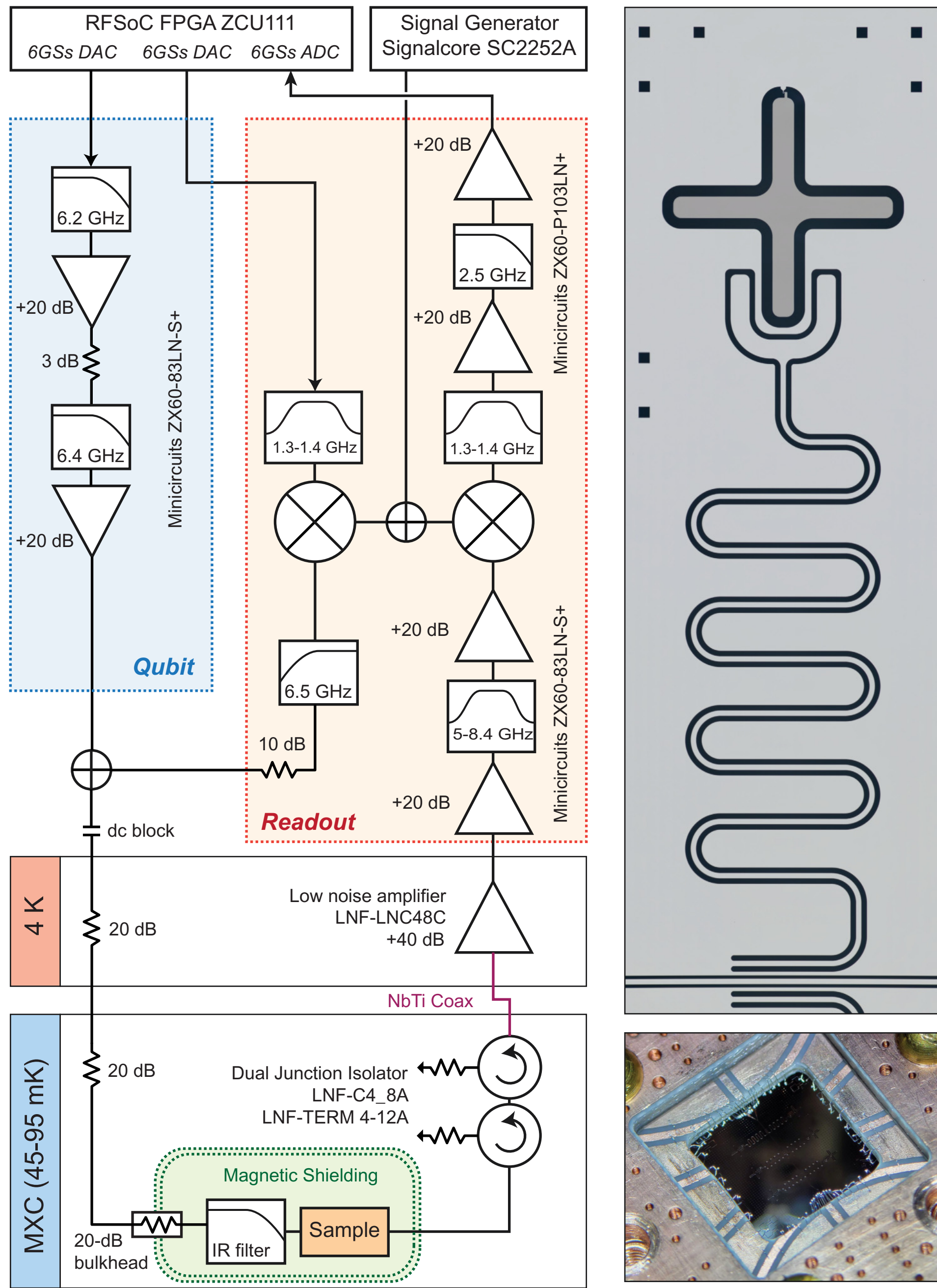

FIG. 12. Schematic of the microwave measurement setup used for qubit characterization. Colored tabs show temperature stages inside the dilution refrigerator. A composite microscope image (top right) shows a single qubit and its readout resonator, coupled to a waveguide for measurement. A photograph (bottom right) shows the chip containing six qubits mounted in its copper circuit board.

turn inductively coupled to a transmission line for readout. For simplicity, we couple directly to the readout resonator without additional purcell filtering. Chips containing up to six qubits and resonators are mounted in a copper circuit board shown in the bottom right of Fig. 12, which is in turn bolted to a copper post thermalizing the assembly to the base temperature of an Oxford Triton 200 dilution refrigerator with minimum mixing chamber temperatures between 45–95 mK. The mounted assembly is encased in two layers of Mu-metal magnetic shielding to reduce decoherence from stray magnetic fields, the qubits are isolated from microwave noise through an Eccosorb CR-110 high-frequency absorbing filter as 60 dB of cryogenic attenuation, which keep the input noise close to the mixing chamber temperature. Transmitted microwave signals pass through two wideband circulators (isolating the qubits from microwave noise from the output side) into a low-loss superconducting NbTi coaxial cable, then are amplified

by a low-noise cryogenic amplifier followed by additional room-temperature amplification.

Resonators and qubit transitions are characterized with single and two-tone spectroscopy using a Agilent E5071C network analyzer. For pulsed qubit measurements, we use a Quantum Instrument Control Kit [79] based on the Xilinx RFSoC ZCU111 FPGA. Qubit pulses are directly synthesized by the FPGA, while measurement pulses are generated with a heterodyne conversion setup, as shown in Fig. 12. With the spectral layout of each device determined, we select filter networks to minimize unwanted images and harmonics from the FPGA for both the qubit and readout pulses, with a broadband example configuration shown in Fig. 12. The FPGA and carrier signal generator are clocked to a 10-MHz rubidium source for frequency stability.

APPENDIX G: MATERIAL LOSS PROBED BY RESONATOR QUALITY FACTOR

To compare qubit-loss contributions from material sources with contributions from the junction itself, we measure quality factors for readout resonators subject to the same fabrication conditions, but with no qubits attached. A typical normalized transmission spectrum of a resonator taken at a low average photon number ($\bar{n}_{\mathrm{ph}} \approx 0.96$) is shown in the inset of Fig. 13(a). On resonance, we observe a dip in magnitude, which at low powers is described well by [80]

$$S_{21} = 1 - \frac{Q}{Q_e^*}\frac{e^{i\phi}}{1 + 2iQ\frac{\omega-\omega_0}{\omega_0}}, \tag{G1}$$

where $Q^{-1} = Q_i^{-1} + \mathrm{Re}[Q_e^{-1}]$ and the coupling quality factor $Q_e = Q_e^* e^{-i\phi}$ has undergone a complex rotation ϕ due to minor impedance mismatches. We plot fitted internal quality factors in Fig. 13(a), finding that Q_i increases with power. This behavior is entirely captured by a power-dependent saturation mechanism [81], suggesting the dominant loss mechanism in the resonators arises from coupling to two-level systems.

We further investigate limits on the resonator loss by using increased temperatures to further saturate the two-level systems. In Fig. 13(b) we plot Q_i measured at $\bar{n}_{\mathrm{ph}} \approx 10^4$ as a function of temperature (grouped by fabrication layer), with solid lines corresponding to a model of the form

$$Q_i(T)^{-1} = Q_{\mathrm{other}}^{-1} + Q_{\mathrm{TLS}}(T)^{-1} + Q_\sigma(T)^{-1}, \tag{G2}$$

where Q_{TLS} is the saturating loss mechanism from two-level systems [81], Q_{other} is a temperature-independent upper bound arising from other sources of loss, and the conduction loss Q_σ is given by [62]

$$Q_\sigma(T) = \frac{1}{\alpha}\frac{\sigma_2(T, T_c)}{\sigma_1(T, T_c)}, \tag{G3}$$

where σ_1 and σ_2 are the real and imaginary parts, respectively, of the complex surface impedance, calculated by numerically integrating the Mattis-Bardeen equations for σ_1/σ_n and σ_2/σ_n [62]. T_c is constrained to the values measured in Appendix B, and α is used as a fit parameter.

Comparing resonators formed during different steps in the fabrication process, we observe that resonators made from the wiring layer exhibit consistently higher quality factors, while resonators from the base layer are lossier and much more variable. Since the sides of the base layer have been exposed to more fabrication steps than the wiring layer, the surface niobium of this layer has a much longer

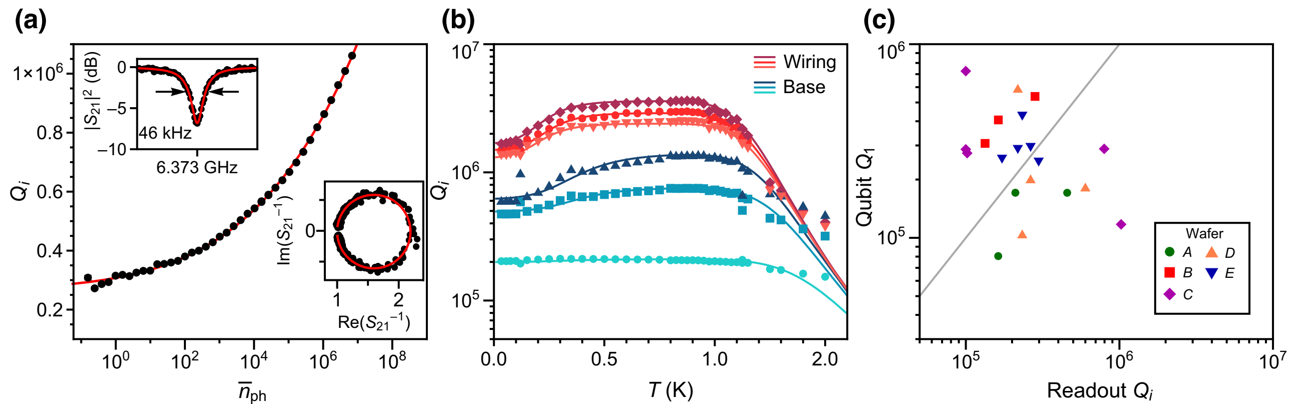

FIG. 13. (a) Power dependence of the internal quality factor for a readout resonator ($Q_e = 2.6 \times 10^5$) with no qubit present. The red line is a fit to a model including loss from two-level systems (TLS). The insets show the lineshape and fits at an average photon occupation $\bar{n}_{\mathrm{ph}} \approx 0.96$. (b) Internal quality factor of resonators without qubits measured as a function of temperature. Solid lines are fits to a model including TLS loss and quasiparticle loss. The three red resonators are formed from the wiring layer, and the blue resonators from the base electrode. Measurements are taken at $\bar{n}_{\mathrm{ph}} \approx 10^4$ so some TLS loss is saturated. (c) Qubit quality factors Q_1 plotted as a function of their readout resonator quality factors Q_i (measured at $n_{\mathrm{ph}} < 1$). A gray line indicates a 1:1 relationship.

chance to oxidize, and has the additional potential to host lossy dielectrics from unremoved spacer material. Thus, while we have improved losses in the wiring layer to about $Q_{\mathrm{TLS}} \sim 0.9 \times 10^6$ by reducing fluorocarbon formation, our devices are still loss limited to approximately 2×10^5 by two-level systems in the surfaces of the base electrode.

To investigate the relationship between qubit and readout resonator decoherence, we also measure quality factors of the readout resonator for each qubit. At single-photon powers, the readout resonator is maximally susceptible to material-based loss from two-level systems in its surface, but due to the hybridization of its electric field with the qubit mode will also interact with the materials in the qubit. In Fig. 13(c) we compare qubit quality factors Q_1 with the single-photon readout quality factor Q_i for each of the devices from Fig. 3. On average, we observe that the two quality factors are close to a one-to-one relationship (as indicated by the gray line), with device variations within a factor of 3 or so. While a direct correlation between the two cannot be extracted from this data, this is to be expected for loss dominated by inhomogeneous material defect distributions between the resonator and qubit. Nevertheless, the similarity of the two quality factors leads us to conclude the qubit and resonator are likely limited by similar decoherence mechanisms.

APPENDIX H: DETAILED MODEL OF JUNCTION LOSSES

In the main text along with Appendix G we established that our junction quality factor ($Q_J \approx 10^5$) is similar to the single-photon quality factors of bare resonators, for which we measured an average of 2.6×10^5 for base layer and 1.04×10^6 for the wiring layer. The fact that these loss rates are comparable suggest that some part of the qubit decoherence arises from the same material losses probed by the resonators. To investigate the origins of these loss channels in more detail and elucidate pathways for further improvement, we use finite-element-method simulations (Ansys HFSS) to examine the energy-participation ratios [61] of different regions and interfaces in the junction.

Figure 14 illustrates the material regions studied. Similar to other surface participation studies [61,81,82] we consider the metal-substrate interface regions, which we further subdivide into the metal-substrate interface (MS) and the dirty metal-substrate region (DMS), which may contain some remaining spacer material. As the etched sapphire surface and bulk loss are both expected to be minimal [83] we combine the substrate-air (SA) interface with the substrate region for participation calculations. Based on the electric field density we choose the thickness of the surface regions of the substrate to be 30 nm: adjusting this thickness will simply rescale the effective participation and loss of the metal substrate regions. The bulk of the loss is expected to lie in the amorphous oxide dielectric regions of the junction. These can be separated into the aluminum oxide comprising the junction barrier (Jox), which we expect to be 1–2 nm [44], and the niobium oxide, which we further separate into a top oxide layer (NbTox) and side oxide (NbSox): the latter of these should be substantially lossier since it may contain fluorocarbons after exposure to the fluorine plasma (see Appendix C). Finally we also consider the possibility of incomplete spacer removal and also include a portion of SiO_2 to model the spacer, as shown in Fig. 14(d). With our imaging methods, we are unable to determine the amount or layout of the residual spacer material, so, for simplicity, we approximate the region as a uniform percentage of the original spacer volume $P_S \leq 1$.

Integrating the simulated electric fields in the junction geometry determines the participation ratios in each dielectric region [61]. The surface niobium oxide thickness t_{NbO_x} typically ranges between 1–5 nm [18,19] but can vary to a greater depending on process conditions, so in Fig. 15(a) we study the participation ratios as a function of t_{NbO_x}. From this we conclude that most of the energy is stored in the junction barrier, followed by the sapphire regions,

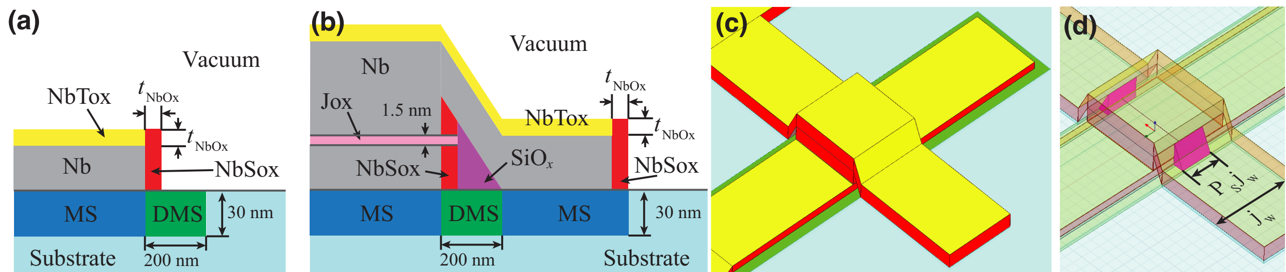

FIG. 14. Junction-loss regions. (a) Sketch showing regions defined for a resonator made with the first layer, with dimensions exaggerated. Niobium oxide (metal-air interface) is separated into top oxide (Tox) and side oxide (Sox) regions. For a wiring layer resonator, the dirty substrate region (DMS) is merged with the substrate layer. (b) Sketch showing regions for a junction, which adds the junction barrier region (Jox) and the spacer region (SiOx). (c) Three-dimensional rendering of the junction with realistic dimensions. Simulated regions are colored in the same way as in parts (a),(b). (d) Transparent rendering of the junction visualizing the spacer remaining percentage P_S relative to the junction width j_w.

with the niobium oxide and spacer regions contributing less than one percent. As expected, the niobium oxide participation increases with t_{NbO_x}, however of note the energy participation is dominated by the side oxide ($p_{\mathrm{Sox}} \gg p_{\mathrm{Tox}}$), especially for thinner values of t_{NbO_x}. In the same manner, we can also simulate the participation ratios of a section of coplanar waveguide [the cross section of which will be the same as that shown in Fig. 15(a)]. Comparing resonators fabricated from the first and wiring layer effectively amounts to the presence of the dirty substrate region (DMS) in our model. For the resonator geometry, we find this region has an average participation $p_{\mathrm{DMS}} = 0.366\%$, largely independent of oxide thickness (for which $p_{\mathrm{NbO}_x} \sim 0.005\%$, similar to Ref. [18]). Based on the single-photon resonator quality factors from both layers in Appendix G, we solve for the material quality factors as a function of the niobium oxide quality factor, which is typically $Q_{\mathrm{NbO}_x} = 1/\tan\delta_{\mathrm{NbO}_x} \simeq 100$ [18,19]. From this we conclude that $Q_{\mathrm{DMS}} \simeq 1.4 \times 10^3$ and $Q_{\mathrm{Sapphire}} \simeq 1.8 \times 10^6$, which is reasonably consistent for averaged bulk and surface measurements of sapphire loss [83] and closer to the loss values found in silicon oxide ($\tan\delta_{\mathrm{SiO}_2} \simeq 2.8 \times 10^{-3}$[84]) in the DMS region.

Combining the expected material losses with the calculated participation ratios, we can express the junction quality factor as a sum of loss contributions from each region to identify dominant sources of decoherence.

$$\tan\delta_J = \frac{1}{Q_J} = \sum_x \frac{p_x}{Q_x} = \sum_x p_x \tan\delta_x. \tag{H1}$$

We summarize the contributions for each material as a function of $t_{\mathrm{NbO}_x} = 2$ nm in Fig. 15(b) along with the average junction quality factors measured in the main text. Despite the high barrier participation, we find the dominant loss contribution is from the niobium oxide: specifically that on the sides of the metal (NbSOx), which is also more likely to be impacted by the plasma-etch chemistry. For simplicity, we have determined the junction barrier quality factor from the average junction quality factor Q_J by assuming that $t_{\mathrm{NbO}_x} = 2$ nm [18] and conservatively estimating $P_S = 0.2$: this yields a junction barrier oxide

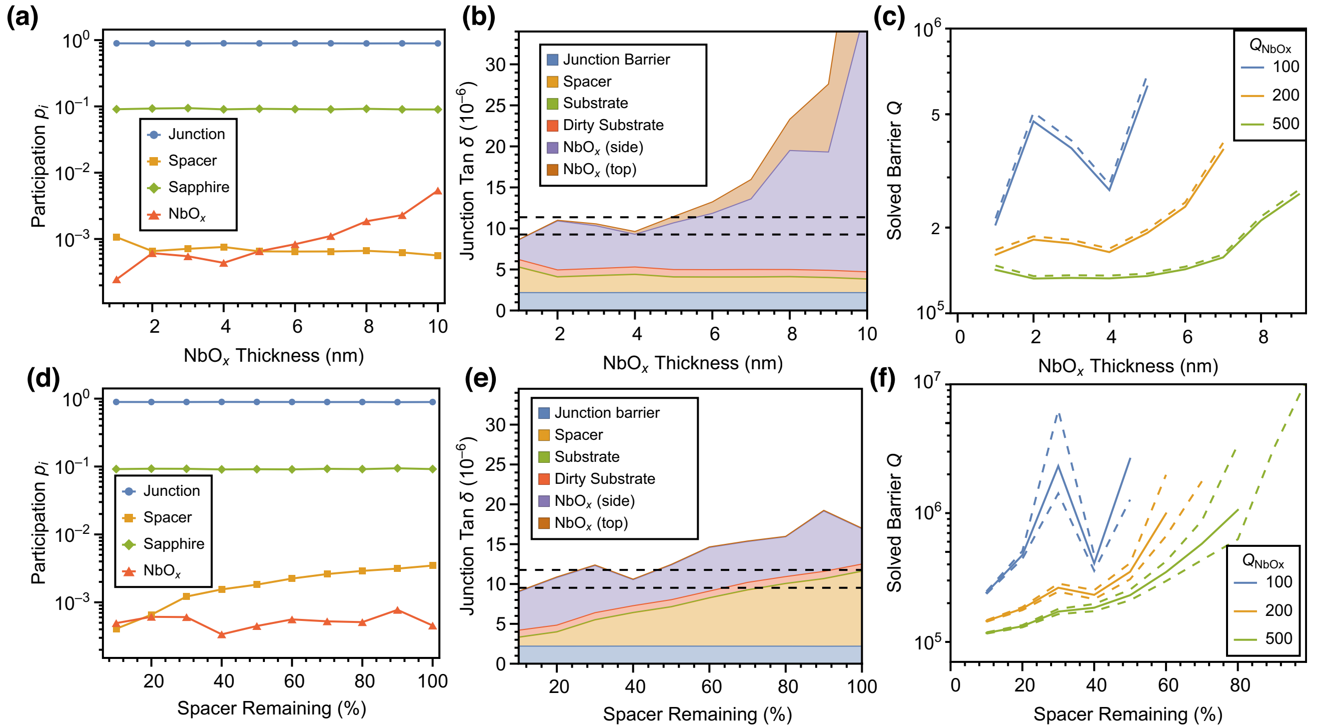

FIG. 15. Junction losses by region. (a) Participation ratios of the primary lossy materials in the junction, plotted as a function of niobium oxide thickness t_{NbO_x}. As expected the niobium oxide participation ratio increases as the layer gets thicker. (b) Junction loss tangent expressed as visual sum of losses from various materials in the junction with assumed loss tangents, plotted as a function of niobium oxide thickness. For thicker oxide layers (e.g., those used in anodization processes) niobium oxide loss dominates the junction loss. The junction loss calculated from Fig. 4(c) is shown in black dashed lines. (c) We can also solve for the barrier quality factor based on the junction quality factor and the calculated participation ratios for varying material quality factors. Solid and dashed lines correspond to a SiO_2 loss tangent of $\tan\delta = 2.7 \times 10^{-3}$ and 2.9×10^{-3}, respectively. In (d)–(f) we repeat parts (a)–(c) but measure the effect of partially unremoved spacer material expressed as a fraction P_S of the junction width. We find that residual spacer material contributes a significant amount of loss. For both sets of simulations, the unswept variable is set to nominal values of $t_{\mathrm{NbO}_x} = 2$ nm and $P_S = 0.2$.

quality factor of $Q_{\mathrm{Jox}} \simeq 4.7 \times 10^5$. We can repeat this calculation with varying conditions to estimate the effective barrier quality, as shown in Fig. 15(c), which suggests that the barrier Q may exceed our estimate if the oxide thickness is thicker than 2 nm, or may be lower if the niobium oxide quality factor is in fact higher than expected. As the predicted junction loss cannot exceed the measured value, assuming standard oxide loss $Q_{\mathrm{NbO}_x} = 100$ [18,19] implies $t_{\mathrm{NbO}_x} < 5$ nm, which helps validate the previous assumptions.

We can also perform a similar set of calculations for the remaining spacer amount P_S, summarized in Figs. 15(d)–15(f). As expected we observe the silicon participation ratio p_{SiO_2} increases with larger spacer volume. When more than half of the spacer remains, we estimate that the silicon oxide comprises the dominant source of loss in the junction. Similar to the niobium oxide thickness, the spacer percentage also affects the estimated junction barrier Q as shown in Fig. 15(f). This also suggests an upper bound for the residual spacer percentage $P_S \lesssim 0.5$, indicating the final wet etch is at least somewhat successful in removing spacer material under the wiring layer.

Thus we have identified several key areas where junction loss could be further improved. As discussed in the main text, reducing the amount of lossy dielectrics (particularly the spacer material and niobium oxide) is key to increasing junction loss, as highlighted in Figs. 15(b), 15(e). While we have taken steps to reduce the volume of both niobium oxides and spacer material, further improvements on both these fronts could help improve junction quality. Further reduction of junction loss may require addressing losses in the dirty-substrate region with improved cleaning methods. However from Figs. 15(a), 15(c) we conclude the junction is most sensitive to the quality of the barrier dielectric. In this regard, atomically uniform barriers such as AlN deposited with molecular beam epitaxy in NbN junctions [27,28] may provide even better performance.

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