Improved Coherence in Optically-Defined Niobium Trilayer Junction Qubits

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Niobium offers the benefit of increased operating temperatures and frequencies for Josephson junctions, which are the core component of superconducting devices. However existing niobium processes are limited by more complicated fabrication methods and higher losses than now-standard aluminum junctions. Combining recent trilayer fabrication advancements, methods to remove lossy dielectrics and modern superconducting qubit design, we revisit niobium trilayer junctions and fabricate all-niobium transmons using only optical lithography. We characterize devices in the microwave domain, measuring coherence times up to 62 µs and an average qubit quality factor above 109: much closer to state-of-the-art aluminum-junction devices. We find the higher superconducting gap energy also results in reduced quasiparticle sensitivity above 0.16 K, where aluminum junction performance deteriorates. Our low-loss junction process is readily applied to standard optical-based foundry processes, opening new avenues for direct integration and scalability, and paves the way for higher-temperature and higher-frequency quantum devices.

A wide variety of superconducting devices have developed on the basis of Josephson junctions: their applications range from quantum-limited amplification and metrology [1, 3] to digital logic [4, 6] and they are an attractive platform for scalable quantum computing architectures due to their design flexibility and wide range of coupling strengths. Increasingly complex and robust quantum circuits have been demonstrated with aluminum junctions [7], however niobium is a tantalizing alternative superconductor due to its larger energy gap (and thus higher critical temperature and pair-breaking photon frequency) [8]. Taking advantage of this wider operating regime, niobium trilayer Josephson junctions became standard for single-flux-quantum circuits operating at liquid helium temperatures [4, 6]. Employing these well-established fabrication processes, some early implementations of superconducting qubits were developed with niobium junctions [9, 10]. However, these initial niobium qubits only retained quantum state coherence for less than 400 ns, diminished by coupling to sources of dephasing and dissipation in the junction and the qubit environment.

Minimizing these loss sources is crucial in all sensitive quantum systems, but particularly for qubits, which must remain coherent over the duration of many gate operations. Significant effort has since been dedicated to investigating and reducing sources of decoherence [17], demanding either adjustments of circuit geometry to limit or dilute coupling to spurious channels, or reducing the use of lossy amorphous dielectric materials. The need for insulated wiring contacts in these niobium trilayer junctions required growing passivating amorphous dielectric material in direct contact with the junction barrier, which likely degraded early qubit coherence [15], and limited their use in quantum devices. Higher temperature junctions with low loss promise a transformative source of strong nonlinearity for high-frequency quantum devices [19, 20], and have since seen renewed interest from efforts to integrate digital and quantum logic [21, 23], and the exploration of tunnel barrier materials beyond the limitations of aluminum [24, 26]. Notably, by removing amorphous insulating scaffolding and increasing the circuit volume to reduce junction participation, qubits with epitaxially grown NbN junctions with crystalline AlN barriers have increased coherence times to 16 µs [27]. We apply similar improvements to traditional Nb/Al/AlOx processes, which are attractive due to the simpler deposition methods required.

In this letter, we use an improved fabrication method to revisit niobium trilayer junctions as the core component of transmon qubits and explore their coherence properties. We describe a method to form a temporary self-aligned sidewall-passivating spacer structure based on Ref. [28], which limits the amorphous spacer material to the smallest necessary region, and can later be chemically removed to further reduce dielectric loss. We find that high-temperature spacer growth methods greatly reduce the critical current density of the junction barrier, allowing us to utilize exclusively optical lithography to fabricate high-nonlinearity junctions for microwave qubits. We find that our all-niobium qubits have lifetimes as high as 62 µs with an average qubit quality factor of 2.57 × 109: much closer to state-of-the-art qubits than past Nb/Al/AlOx devices [9-14]. We further observe that the higher superconducting gap energy results in reduced sensitivity to quasiparticles, particularly above 160 mK, where conventional aluminum-junction qubit performance deteriorates. These results demon-
strate the reemergent relevance of niobium junctions for pushing the boundaries of superconducting devices.

Despite niobium’s attractive electrical properties, in thin layers its oxides are imperfect insulators with high dielectric loss [18], resulting in very poor natural tunnel junction barriers. Aluminum, on the other hand, forms a thin self-terminating oxide with low leakage and loss, but has a low critical temperature. The trilayer method leverages the strengths of both of these materials by using a thin layer of oxidized aluminum as the tunnel barrier and encapsulating it with niobium: through the proximity effect the Josephson junction inherits desired electrical properties and a clean tunnel barrier. This trilayer structure is typically grown on a wafer-scale as the first step in fabrication, enabling excellent uniformity [29, 30] and high purity growth methods.

Our fabrication process (see Appendix A) is illustrated in Fig. 1. Similar to methods using sputtering, our trilayer is formed in a shadow-evaporation-compatible electron-beam system by depositing 80 nm of Nb and 8 nm of Al on high-purity single-crystal sapphire that has been annealed and chemically etched to remove surface damage. The deposition rate is kept high to maximize film quality (see Appendix B). To reduce defects and promote aluminum oxide formation [31], the aluminum is first ion milled then oxidized with an O₂-Ar mixture. To prevent oxygen diffusion into the Nb layer and the formation of lossy NbOₓ [18, 22], the oxidized Al surface is protected by a thin (3 nm) capping layer of Al. This layer is deposited while rotating the substrate at an angle for complete coverage while keeping it thin enough to avoid affecting junction properties. A (150 nm) thick counter electrode is then deposited on top, forming the trilayer in-situ, without breaking vacuum.

The trilayer is patterned with I-line [33] photolithography and plasma-etched in one step with Cl₂, BCl₃ and Ar to define the bottom electrode (Fig. 1b). As it is necessary to make contact to the counter electrode without touching the base electrode, we then form an insulating sidewall-passivating spacer structure [28]. Amorphous SiO₂ is grown isotropically (Fig. 1c) by either plasma-enhanced chemical vapor deposition (PECVD) which heats the wafer to 300 °C for 16 min or high density plasma-enhanced chemical vapor deposition (HDPCVD) (90 °C). The SiO₂ is now etched anisotropically with a highly directional CF₄, CHF₃, and Ar plasma, which forms the spacer structure when the bulk material has been etched away (Fig. 1d). The contaminated trilayer surface is ion milled, and the 160 nm Nb wiring layer is electron-beam-deposited on the sample (Fig. 1e). We verify that this forms a low-resistance contact to the counter electrode (see Appendix B).

The wiring layer is patterned and a selective SF₆, CHF₃, O₂ and Ar plasma etch removes the wiring layer and the counter electrode, defining the perpendicular top junction electrode (Fig. 1f). This etch is carefully optimized to minimize the formation of lossy fluorocarbon polymers [34] (see Appendix C) while preserving chemical selectivity: and although the plasma etches the Al layers far slower than Nb, the etch is still timed to finish a few seconds after the counter electrode is fully removed to limit excessive polymer deposition. Finally, to further remove the lossy amorphous materials present in the junction, a solution of NH₄F and acetic acid [35] are used to dissolve the remaining SiO₂: this process additionally removes any exposed Al and a small amount of surface NbOₓ (Fig. 1g). As this step can dissolve aluminum in the junction as well, etch times are kept below 15 s. This final treatment could likely be improved with a HF vapor etch, which has shown good results forming...
similar contact structures [36].

We verify the expected Josephson junction behavior [37] in our devices by measuring their hysteretic current-voltage curves in Fig. 2a. When cooled to 860 mK, the un-shunted junction shows a zero-resistance superconducting branch up to the critical current $I_c$, and an energy gap $2\Delta = 5.64$ meV, corresponding to a critical temperature $T_c = 9.2$ K, in agreement with the transition temperature seen in resistivity measurements. Measuring the asymptotic normal state resistance $R_n$ above the energy gap we find a $I_c R_n$ product of 1.5 mV, similar to values reported previously for Nb trilayer junctions [28–30, 35, 53]. Although measurements of the subgap region were limited by the experiment hardware, no excessive subgap leakage currents are observed.

Using the $I_c R_n$ product found above, we can use room-temperature junction resistances to predict low-temperature properties [39, 41]. Fitting the measured resistance for junctions of varying areas with two free parameters, specific resistivity and junction critical dimension bias (see Appendix D), we obtain the effective junction areas and the specific critical current density $J_c$ for each wafer. This method allows us to easily investigate effects of the fabrication process on junction electrical parameters. For Nb trilayers, the critical current density is sensitive to temperature [38] as well as oxygen exposure $E$, the product of oxygen partial pressure and oxidation time: this relationship has been empirically found to match $J_c \propto E^{-0.5}$ [28, 39, 42, 43]. In Fig. 2b, we plot $J_c$ as a function of $E$ for wafers with trilayers grown using various oxidation parameters and fabricated with two spacer deposition methods. For the HDPCVD junctions, we find critical current densities in the kA cm$^{-2}$ range, comparable with other methods [28, 38, 39, 45], and observe reasonable agreement with the oxygen exposure dependence described above. The effect of process temperature is readily apparent when we examine junctions with high-temperature-grown PECVD spacers: compared to HDPCVD junctions, we observe nearly a factor of 50 reduction in $J_c$. We find this temperature-annealing effect activates above 200°C (see Appendix F), in agreement with [48], and is likely the result of reduced barrier transparency [49] from diffusion.

With access to a wide range of $J_c$, we can use PECVD-annealed junctions to realize qubit junctions with optical lithography. We fabricate microwave transmon qubits [42, 48] with a standard geometry (see Appendix E) capacitively coupled to a coplanar waveguide resonator for dispersive readout. The qubit capacitor, ground plane and readout resonator are defined on either the base electrode or wiring layer, so no additional fabrication steps are needed. Chips with several qubits and their readout resonators sharing a common microwave feedline are characterized at the base stage of a dilution refrigerator (45–95 mK). Using microwave spectroscopy [47], we verify our qubits have anharmonicities around 140 MHz, and couple with strengths of 30–60 MHz to their readout resonators.

For superconducting qubits, the relaxation time and dephasing time are parameters of particular interest, as they dictate qubit limitations and act as sensitive probes for loss channels. We measure relaxation time by placing each qubit in its excited state and measuring it after time $t$: fitting the exponential decay gives the characteristic time $T_1$. We perform these measurements for each qubit and show averaged results as a function of qubit frequency in Fig. 3a, finding $T_1 = 62.4$ µs for our best device. To probe loss channels in detail we use the frequency-independent qubit quality factor $Q_1 = \omega_c T_1$, which we find for our devices is on average above $10^6$: within an order of magnitude of recent aluminum qubits [7, 49, 52] and similar to readout resonator quality factors (see Appendix G). We also perform a Ramsey experiment to measure the dephasing time $T_2^*$ and a Hahn-echo experiment to characterize the spin-echo dephasing time $T_2$. We find that $T_2^*$ is within a factor of 2 of $T_1$, and particularly limited at lower qubit frequencies, where the environment two level system (TLS) temperature is higher and system $1/f$ noise is higher. The $T_2$ values, which decouple low frequency noise are noticeably higher, demonstrated in particular by the qubits below 2 GHz from wafer B, suggesting that more careful filtering and environment control could reduce dephasing further.

To assess loss contributions from the junction independent of other sources, in Fig. 3b: we use the increased junction participation ratio $p_j = c_j/C_j$ [49, 58] in our devices to examine the effects on $Q_1$. For our devices (red), we estimate an effective junction quality factor of $10^5$: approximately 100 times greater than previous Nb/Al/AlO$_x$ qubits (blue) [9, 10], and much closer to epitaxial NbN junctions (black) [25, 27] and modern
aluminum-junction qubits (green) \[29,22\]. Extrapolating to lower \( p_j \) values, we find our device loss is largely not limited by the junction, indicating that material refinements and device engineering could further improve qubit performance.

Next we investigate our qubits at increased operating temperatures, shown in Fig. 4. We observe a mild decrease in \( T_1 \) with temperature above 160 mK, consistent with heating from the environment bath \[14\], but importantly don’t see the drastic temperature dependence expected for quasiparticle-induced loss \[54\], in line with expectations for niobium. The advantage of higher-temperature junctions is apparent when comparing our qubit performance to an aluminum counterpart: above 160 mK, the aluminum qubit is quickly overwhelmed with quasiparticle-induced decoherence, whereas our devices largely retain their properties.

We have described a Nb/Al/AIO\(_x\)/Al/Nb trilayer fabrication method demonstrating a 100-fold improvement in junction loss at the single-photon level. By removing lossy dielectric materials wherever possible, we use our low current density junction process to fabricate microwave transmon qubits using I-line photolithography demonstrating quasiparticle quality factors within an order of magnitude of recent aluminum devices. Our qubits have relatively high junction participation ratios, which could either be reduced to improve coherence through material optimization \[18\], or exploited further to significantly reduce qubit size \[21,49\]. Together with this device footprint flexibility, our all-optical qubit process opens the door to large-scale direct integration of scalable quantum processors with digital superconducting logic \[21,28\]. Niobium’s higher energy gap significantly reduces sensitivity to quasiparticles for our junctions compared to aluminum analogues, allowing operation at much higher frequencies, and resulting in far less decoherence above 160 mK where conventional qubit properties deteriorate. Combined with their low loss, these properties make our trilayer junctions a promising candidate for quantum architectures with lower cooling power requirements, hybrid qubit systems requiring elevated temperatures, and enable new possibilities for nonlinear elements at millimeter-wave frequencies \[19,20\], paving the way for higher temperature, higher frequency quantum devices.

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[33] Exposed with a 375 nm laser.
[61] L. Stefanazzi, K. Treptow, N. Wilcer, C. Stoughton,


Appendix A: Fabrication Methods

<table>
<thead>
<tr>
<th>Etch 1 (Fig. 1b)</th>
<th>T(°C)</th>
<th>Pressure</th>
<th>ICP/Bias Power</th>
<th>Cl2</th>
<th>BC13</th>
<th>Ar</th>
<th>CF4</th>
<th>CHF3</th>
<th>SF6 (O2)</th>
<th>etch time (s)</th>
<th>etch rate (nm/s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>20 ± 0.1</td>
<td>5 mT</td>
<td>400 W / 50 W</td>
<td>30</td>
<td>30</td>
<td>10</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>120-140 s</td>
<td>~ 4.5 nm/s</td>
<td></td>
</tr>
<tr>
<td>Etch 2 (Fig. 1c)</td>
<td>20 ± 0.1</td>
<td>30 mT</td>
<td>500 W / 60 W</td>
<td>-</td>
<td>10</td>
<td>30</td>
<td>20</td>
<td>-</td>
<td>65-90 s</td>
<td>~ 2 nm/s</td>
<td></td>
</tr>
<tr>
<td>Etch 3 (Fig. 1d)</td>
<td>20 ± 0.1</td>
<td>5 mT</td>
<td>400 W / 60 W</td>
<td>-</td>
<td>7</td>
<td>-</td>
<td>40</td>
<td>4</td>
<td>50-60 s</td>
<td>~ 4.5 nm/s</td>
<td></td>
</tr>
</tbody>
</table>

TABLE I. Plasma etch parameters used in the ICP-RIE etches described in the process. Etches are performed in an Apex SLR ICP etcher. Gas flows are listed in sccm.

C-plane polished sapphire wafers are ultrasonically cleaned in toluene, acetone, methanol, isopropanol and de-ionized (DI) water, then etched in a piranha solution kept at 40°C for 2 minutes and rinsed with de-ionized water. Immediately following, the wafers are loaded into a Plassys MEB550S electron-beam evaporation system, where they are baked at >200°C under vacuum for an hour to help remove water and volatiles. When a sufficiently low pressure is reached (< 5 × 10⁻⁸ mbar), titanium is electron-beam evaporated to bring the load lock pressure down even further. The trilayer is now deposited by first evaporating 80 nm of Nb at > 0.5 nm/s while rotating the substrate. After cooling for a few minutes, 8 nm of aluminum is deposited while rotating the substrate at a shallow angle (10 degrees) to improve conformality. The aluminum is lightly etched with a 400 V Ar⁺ beam for 10 s, then oxidized with a mixture of 15% O₂:Ar at a static pressure. After pumping to below (< 10⁻⁷ mbar), titanium is again used to bring the vacuum pressure down to the low 10⁻⁸ mbar range. We note that the pressure for the remainder of the trilayer deposition is higher than for the first Nb layer. The second 3 nm layer of Al is evaporated vertically while rotating the substrate to minimize void formation in the following layer. The counter-electrode is then formed by evaporating 150 nm of Nb at > 0.5 nm/s. The substrate is allowed to cool in vacuum for several minutes, and we attempt to form a thin protective coating of pure Nb₂O₅ by briefly oxidizing the top surface at 3 mbar for 30 s.

The wafers are mounted on a silicon handle wafer using AZ1518 photoresist cured at 115°C, then coated with 1 µm of AZ MiR 703 photoresist and exposed with a 375 nm laser in a Heidelberg MLA150 direct-write system. The assembly is hardened for etch resistance by a 1 min bake at 115 °C then developed with AZ MIF 300, followed by a rinse in DI water. The entire trilayer structure is now etched in a chlorine inductively coupled plasma reactive ion etcher (Etch 1 in Table I). The plasma conditions are optimized to be in the ballistic ion regime, which gives high etch rates with minimal re-deposition. Immediately after exposure to air, the wafer is quenched in DI water: this helps prevent excess lateral aluminum etching by quickly diluting any surface HCl (formed by adsorbed Cl reacting with water vapor in the air). The remaining photoresist is thoroughly dissolved in a mixture of 80°C n-methyl-2-pyrrolidone with a small addition of surfactants, which also removes the substrate from the handle wafer.

The wafer is ultrasonically cleaned with acetone and isopropanol, then SiO₂ spacer is grown by either HDPCVD or PECVD. For PECVD, SiH₄ and N₂O are reacted in a 100 W plasma with the chamber at 300°C. The complete process (including chamber cleaning pumping and purging steps) takes approximately 15 minutes. For HDPCVD, the wafer is mounted on a silicon handle wafer using Crystalbond 509 adhesive softened at 135 °C, then the spacer is deposited with a SiH₄ O₂ and Ar plasma, with the substrate heated to 90 °C. The wafers are now etched in a fluorine reactive ion etch (Etch 2 in Table I). This etch is optimized to be directional but in the diffusive regime to promote chemical selectivity while enabling the formation of the spacer structure. At this point minimizing oxide formation is crucial since the top surface of the trilayer is exposed and will need to form a good contact to the wiring layer, so immediately following the completion of the etch, wafers are separated from the handle wafer by heating to 135 °C, ultrasonically cleaned of remaining adhesive in 40°C acetone and isopropanol, then immediately placed under vacuum in the deposition chamber, where they are gently heated to 50 °C for 30 min to remove remaining volatiles.

The contaminated and oxidized top surface of the counter electrode is etched with a 400 V Ar⁺ beam for 5 min, which is sufficient to remove any residual resistance from the contact. After pumping to below (< 10⁻⁷ mbar), titanium is used to bring the vacuum pressure down to the low 10⁻⁸ mbar range. The wiring layer is now formed by evaporating 160 nm of Nb at > 0.5 nm/s. The substrate is allowed to cool in vacuum for several minutes, and the wiring layer is briefly oxidized with 15% O₂:Ar at 3 mbar for 30 s to promote a thin protective coating of pure Nb₂O₅. The wafers are again mounted on a handle wafer, coated with AZ MiR 703 photoresist and exposed with a 375 nm laser. The assembly is hardened for etch resistance by a 1 min bake at 115 °C before development. The final structure is now defined with a fluorine reactive ion etch (Etch 3 in Table I). This step proves to be highly problematic as it easily forms inert residues, and needs to be highly chemically selective in order to avoid etching through the aluminum, so the plasma is operated in a low-density ballistic regime with the addition of O₂ which helps passivate exposed aluminum and increase selectivity. The etch time is calculated for each wafer based on visual confirmation when the bare wiring layer is etched through. We remove crosslinked polymers from the photoresist surface with a...
mild 180 W room temperature oxygen plasma that minimally oxidizes the exposed Nb (though find this is not very effective). The remaining resist is now fully dissolved in 80°C n-methyl-2-pyrrolidone with surfactants.

With the junctions now formed, the wafer is ultrasonically cleaned with acetone and isopropanol, coated with a thick protective covering of photore sist (MiR 703) cured at 115°C, and diced into 7 nm chips. The protective covering is now dissolved in 80°C n-methyl-2-pyrrolidone with surfactants (we find this can also help remove stubborn organic residues from previous steps), and the chips are given a final ultrasonic clean with with acetone and isopropanol. The remaining silicon spacer is now dissolved by a short 10-15 s etch in a mixture of ammonium fluoride and acetic acid (AlPAD Etch 639), quenched in de-ionized water, then carefully dried from isopropanol to preserve the now partially suspended wiring layer. The finished chips are packaged and cooled down within a couple hours from this final etch to minimize any NbOx regrowth from air exposure.

Appendix B: Junction Superconductor Properties

![Graphs](image)

**FIG. A1.** Superconductor material quality. (a) Niobium superconducting critical temperature $T_C$ extracted from resistivity measurements as a function of metal deposition rate. At rates above 0.6 nm/s, $T_C$ approaches bulk value (dashed line). The inset shows deviations from bulk $\Delta T_C = T_C^{\text{bulk}} - T_C$ are correlated with the residual resistivity ratio, implying high deposition rates result in high-quality films. (b) Sheet kinetic inductance $L_k$ and observed London penetration depth $\lambda_L$ plotted as a function of deposition rate suggesting that films deposited at higher rates are closer to the clean superconductor limit. (c) Specific junction resistance $R_J = R/N$ obtained by measuring the resistance $R$ of a chain of $N = 12$ junctions as a function of temperature. A sharp drop in resistance is observed above 9 K as the niobium electrodes begin to superconduct. As the temperature decreases, the junction critical currents increase above the excitation current (10 μA), and below 5 K the measured resistance drops to zero as the excitation is confined to the superconducting branch, indicating proximitization of the aluminum and superconducting contact between the counterelectrode and wiring layers.

Josephson junction properties are largely determined by the characteristics of the two superconductors and the insulating oxide barrier that separates them, so the initial formation of the trilayer materials is crucial for the device quality. As niobium sets the limit of superconducting properties and losses in our junctions and qubits, it is crucial to begin with a high-quality and thus high-purity material. Maintaining material purity presents a challenge for any thin film deposition technique, made difficult in particular by the incorporation of contaminants into the film during growth. This contamination can be addressed with two main approaches: first by reducing the flux of contaminants (achieved by reducing the vacuum pressure during the deposition process), but also by reducing the duration of exposure, which can be controlled by the deposition rate.

For electron beam evaporation (the deposition technique used here) vacuum pressures are reduced as low as possible during deposition, however are limited to the $10^{-8}$ mbar range by the hardware. With the contaminant flux fixed by the deposition system vacuum pressure, we explore the effect of deposition rate on Nb purity. By measuring the resistivity of a film with a known geometry at varying temperatures, we obtain a wealth of information about the film properties. In Fig. [A1](image) we plot the superconducting transition temperature $T_C = \Delta_0/1.76k_B$ (proportional to the superconducting gap $\Delta_0$) as a function of metal deposition rate. We observe that higher rates yield increased transition temperatures, which approach those found in bulk high-purity Nb [55], indicating that the films are increasingly pure. Indeed, we can also correlate the residual resistivity ratio $\text{RRR} = \rho(300 \text{K})/\rho(T_C)$, an indicator of superconductor quality, with deviations of measured critical temperature the bulk value $T_C^{\text{bulk}}$, supporting the notion that higher deposition rates yield higher-quality films. Due to the extreme local temperatures required, practical considerations and stability concerns put a limit on feasible deposition rates. Nonetheless, despite variations induced by vacuum conditions, we find that rates above 0.6 nm/s are required to deposit a film with high purity.
We can go further to examine the degree of disorder in the superconductor by probing the kinetic sheet inductance
\[ L_K = \frac{\hbar R_\square}{\pi \Delta_0} \]
where \( R_\square = \rho_0/t \) is extracted from the film thickness \( t \), and the resistivity just above the superconducting transition. The sheet inductance also yields the London magnetic penetration depth \( \lambda_L^2 = \frac{t L_K}{\mu_0} \). In Fig. A1 we find that both \( L_K \) and \( \lambda_L \) are also reduced with films deposited at higher rates. Lower kinetic inductance and shorter London lengths indicate a lower degree of disorder in the superconductor, suggesting that increased deposition rates bring the material further away from the disordered dirty superconductor limit \( (\lambda_L > \xi) \) [56].

We verify the superconducting contact quality between the wiring layer and the counter-electrode, as well as the junction tunnel barrier transparency by measuring the voltage across a chain of 12 junctions in series, through which we send a fixed excitation current of 10 \( \mu \)A. In Fig. A1c we plot the per-junction specific resistance \( R_J \) as a function of temperature, showing the immediately apparent superconducting transition above 9 K. Immediately below the transition, the superconducting gap is still relatively low, and the junction critical currents fall below the excitation current, so a small resistance is observed. However as we decrease the temperature, we find that the resistance shrinks by several orders of magnitude (below the noise floor of the instrument). This indicates that the sum of any remaining resistance channels in a single junction is likely well below the m\( \Omega \) range, suggesting a superconducting contact between the Nb wiring layer and the Nb counter-electrode.

**Appendix C: Lossy Plasma Etch Residues**

**FIG. A2.** Etch residue chemical analysis. (a) Scanning electron micrograph of a plasma etch residue located on the wiring layer near a junction. (b) Composite Energy Dispersive Spectroscopy (EDS) image overlaid on the image in (a) showing normalized element density regions for F, Nb, Al, and O, with individual element density maps shown in their respective color on the right. Along with clear Nb and sapphire \( (\text{Al}_2\text{O}_3) \) regions, a high concentration of fluorine relative to the background is found in the residue region, suggesting the residue is composed of fluorinated polymers.

By virtue of size, the electric field concentration in a junction is orders of magnitude higher than in the qubit capacitor (or any planar structure such as the resonator capacitor), meaning the participation ratio [53] of the junction side surfaces will also be much higher. As such, our junction loss is likely still limited by the presence of lossy dielectrics formed on the sides of the junction, which for our design are primarily either spacer material, metal oxides, or residues left by the reactive ion etching process. As we cannot use more aggressive spacer [36] or oxide removal methods [18] without further risking the integrity of the aluminum junction barrier, we instead study the etch residues and discuss mitigation strategies.

Alongside the desired chemical and mechanical processes that remove niobium, reactive ion etching hosts a variety of simultaneous mechanisms that can grow material: etched material can either be re-deposited by sputtering, low-energy reaction products can re-adsorb onto exposed surfaces, and components in the plasma can react with exposed material [34]. The products of all of these mechanisms tend to be much more difficult to remove, so end up staying behind after the photoresist is dissolved, particularly on vertical walls not directly exposed to plasma bombardment during the etch. While the deposited material passivates the walls of the etched region during the etch and can produce high-aspect ratio features, for our junctions its critical to reduce any excess dielectrics, so we explore ways to understand and mitigate these residues in order to reduce loss.

In Fig. A2 we show an example of a dielectric residue located on the side of a junction, which has not been removed throughout the entire fabrication process. This material must be formed during the third dry etch (Fig. I) since it covers and extends off the sides of the Nb wiring and counter-electrode layers. The residues appear to be present on all vertical surfaces exposed by the etch, visible as striations on the junction sides. To determine the deposition mechanism for this residue, we probe the chemical composition of the residue using energy dispersive spectroscopy (EDS). A composite map of normalized element composition is overlaid on the same image of the residue in Fig.
with individual normalized element concentration maps shown to the right. As expected, we observe high Nb concentrations in the metal regions, and high aluminum and oxygen concentrations in the sapphire region, but more importantly we observe a significant concentration of fluorine in the residue (carbon is also observed in this region as well, but cannot be quantified due to high background carbon levels). This heavily suggests the residue is some kind of fluorocarbon polymer.

Fluorocarbons are chemically inert and robust against most standard solvents, acids, or oxygen plasma, and the residues remain largely unaffected by these conditions. However, fluorocarbon polymers are susceptible to defluorination by strong alkali reductants such as sodium-potassium amalgam (NaK) [57, 58]. In Fig. A3, we show a device with particularly extensive residues covering and extending off the sides of the wiring layer. In an oxygen-free dry nitrogen glovebox, we immerse the sample surface in a sodium-potassium amalgam (NaK) for 15 min, rinse with tetrahydrofuran, move the sample into air, finish rinsing with acetone and isopropanol, then image the residues. In Fig. A3c we observe that the residue material is largely removed: the overhanging features have been removed, as well as the material on metal sides, with the original extent of the residue (about 30 nm) apparent by the indentation left on the sapphire by the residue during the etch. This corroborates the hypothesis that these residues are composed of fluorocarbons, since the material could be removed upon treatment with NaK, wherein the amalgam cleaves the problematic C-F bonds and allows the remaining residues to become soluble in organic solvents.

While this NaK treatment appears promising on the microscopic scale, in practice the amalgam is difficult to keep clean, and leaves behind significant quantities of dust and salt deposits on the chip surface. A more practical method to post-clean any residues left behind by the etch might be to instead use a solution with a high reducing potential such as sodium-napthalenide [57], commonly used as a surface treatment for PTFE. Regardless, the best way to remove the residues is to not form them in the first place, which is achieved by optimizing the etch plasma conditions. First, we remove obvious residue sources by ensuring the plasma chamber is thoroughly cleaned with oxygen, and no fluorinated vacuum oils are present in the system. We find that using gas constituents with low hydrogen and carbon content (eg. SF$_6$ or CF$_4$) significantly reduces the residue growth: in particular we find CHF$_3$ and C$_4$F$_8$ readily polymerize. However, we note that using too much SF$_6$ can lead to the incorporation of sulfur [59] into any exposed SiO$_2$, which forms an even more inert residue and should be avoided. The addition of O$_2$ in the plasma can also help increase the carbon-fluorine ratio of the plasma [60], but also increases resist etch rate and passivates exposed metal. Using a low density plasma with a long mean free path for the radicals is key to increasing the etch rate and reducing re-deposition, as it increases the effective reactant and product temperature. Residue formation is also particularly sensitive to substrate temperature. With the substrate too cold, the reaction product temperature becomes low enough to allow recondensing, leading to increased fluorocarbon deposition. If the substrate is too hot, reactivity of the photoresist polymers is increased, promoting crosslinking, polymerization, and fluorination: thus good thermal contact between the substrate and the carrier wafer is essential, as the high temperature plasma can otherwise significantly heat the substrate. Finally, we observe the residue formation accelerates when the insulating substrate is exposed (likely a result of screening charges focusing the plasma towards remaining metal), so we ensure the etch is stopped within 15s of completion.
APPENDIX D: JUNCTION AREA DEPENDENCE

Having verified the relationship between the normal state resistance $R_n$, the critical current and the gap energy [11] (see Fig. 2), we can use room temperature resistance measurements to efficiently predict cryogenic junction properties. In Fig. 4a, we show room temperature junction resistance and junction inductance (calculated from resistance using the $I_J R_N$ product), plotted as a function of junction area (corrected for lithographic reduction). The original un-treated (see Fig. 1) junction resistances are in good agreement with the expected inverse dependence on junction area, enabling us to fit the original critical current density. After etching the spacer (see Fig. 1k) some of the aluminum is removed as well, and the resistance increases since the effective junction dimensions have shrunk. By fitting the etched junctions, we extract an dimension reduction of approximately 160 nm, which corresponds to about 80 nm of aluminum that gets removed by the etch. We note that this sets a practical limit on how small the junction can be before etch effects become more significant than lithographic definition of junction area.

Fitting junction resistances as a function of the final junction area (taking into account the dimension reductions) yields the true critical current density for the final junctions (Fig. 4b). We repeat these measurements for wafers with different processing conditions to populate Fig. 2. A spread (typically between 5-10%) is noticeable in our junction resistance for a given junction area. While higher than typical niobium trilayer junction non-uniformity [29, 30], our junction variance can primarily be attributed to relatively large geometric deviations due to the limits of our lithographic resolution, which is compounded by fluctuations in the etch dynamics that determine the final junction area. Because of this we cannot probe the uniformity of the trilayer barrier itself, however estimate that it behaves similarly as in other trilayer junctions investigated, implying that our junction parameter spread could likely be reduced with higher resolution lithography methods and a more selective spacer removal technique. We test the functional limits of our junction reproducibility by measuring deviations of qubit frequencies across different chips from different wafers. In Fig. 4c, we show qubit frequencies (determined by junction inductance) as a function of design junction area for devices with two different qubit capacitor designs. After determining the qubit capacitance and applying the estimated junction area reductions, we find the measured frequencies are self-consistent within 10 percent or so, even across separate wafers.

APPENDIX E: JUNCTION ANNEALING MECHANISM

The effect of process temperature is readily apparent when comparing the resulting critical current densities of junctions with PECVD spacers (deposited at 300 °C) and those with HDPCVD-grown spacers (90 °C). In Fig. 2b, for the high temperature PECVD junctions, we observed an approximately 2.3% reduction in $J_c$. We investigate this effect in more detail by annealing finished low temperature (HDPCVD) junctions with initial $J_c \sim 3 \text{kA cm}^{-2}$ in a dry Ar atmosphere, then re-measuring their critical current density. In Fig. 5a, we plot the annealed $J_c$ as a percentage of the untreated $J_c$, and confirm that the annealing effect activates above 200 °C, in agreement with [35]. In Fig. 5b, we show the critical current density of junctions annealed
at 300 °C for various lengths of time. After about 20 min (the approximate time wafers spend at 300 °C during PECVD) we find that the current density reduction approaches the measured ratio between the PECVD and HDPCVD junctions. This suggests the high-temperature process dynamically anneals the junction barrier, likely increasing mobility and in the oxide barrier which enables diffusion and reduces pinhole density [46]. Qualitatively, this process appears to be exponential in time, so we overlay a saturating exponential fit of the form $J_c/J_{c0} = (1 - \alpha)e^{-t/\tau} + \alpha$, where $\alpha$ is the observed reduction factor, and obtain a critical time $\tau \approx 4$ min. The observed annealing effect is consistent with the critical current densities measured in Ref. [28] which do not exceed 190 °C during the fabrication process. With this in mind, our PECVD process could be modified to produce high critical current density junctions by either reducing the deposition temperature below 200 °C or to a lesser extent by limiting the time spent at elevated temperatures.

Appendix F: Qubit Geometry and Experimental Setup

The qubit, readout resonator and other structures are formed in the same steps as the junction. We base our design on a qubit geometry [48] popular for it’s reduced radiation profile, a result of the cross-shaped coplanar qubit capacitor whose local electric dipole moments act to cancel each other out far away. In our case, the cross shape (typically used to implement qubit-qubit coupling or additional charge drives) isn’t strictly necessary and a coplanar capacitor composed of any two-dimensional shape would work as well. We also make an effort to minimize coupling to lossy two-level systems in surface dielectrics by rounding sharp corners where possible in the geometry. This reduces electric field concentration at specific points in the capacitor, leaving a weaker and more homogenous electric field which should couple less strongly to individual two-level systems.

An example of our qubit geometry is shown in a composite microscope image on the top right of Fig. A6, imaged after Etch 3 (Fig. 1f). The niobium and un-etched aluminum have visibly different colors, allowing us to distinguish between the wiring layer and the base electrode. In our geometry, the qubit capacitor is formed with both layers, while the rest of the circuit and the majority of the chip (ground plane, readout resonator and coupling waveguides) is formed with just one layer. We find that the wiring layer readout resonators exhibit lower loss (See Appendix G), so typically pick the wiring layer for the ground plane. However having measured devices with both configurations (majority wiring layer and majority base electrode), we don’t find extreme differences in qubit properties, where the fields participate in both layers regardless of orientation. As an example, compare base-electrode ground plane wafer D with wiring ground plane wafer A in Fig. 3a, whose qubit quality factors are similar.

The qubits are capacitively coupled to a meandered quarter wave coplanar waveguide resonator, which is in turn inductively coupled to a transmission line for readout. For simplicity, we couple directly to the readout resonator without additional purcell filtering. Chips containing up to 6 qubits and resonators are mounted in a copper circuit board shown in the bottom right of Fig 1a which is in turn bolted to a copper post thermalizing the assembly to the base temperature of an Oxford Triton 200 dilution refrigerator with minimum mixing chamber temperatures between 45–95 mK. The mounted assembly is encased in two layers of Mu-metal magnetic shielding to reduce decoherence from stray magnetic fields, the qubits are isolated from microwave noise through an Eccosorb CR-110 high-frequency absorbing filter as 60 dB of cryogenic attenuation which keep the input noise close to the mixing chamber temperature. Transmitted microwave signals pass through two wideband circulators (isolating the qubits from microwave noise...
FIG. A6. Schematic of the microwave measurement setup used for qubit characterization. Colored tabs show temperature stages inside the dilution refrigerator. A composite microscope image (top right) shows a single qubit and its readout resonator, coupled to a waveguide for measurement. A photograph (bottom right) shows the chip containing 6 qubits mounted in its copper circuit board.

from the output side) into a low-loss superconducting NbTi coaxial cable, then are amplified by a low noise cryogenic amplifier followed by additional room temperature amplification.

Resonators and qubit transitions are characterized with single and two-tone spectroscopy using a Agilent E5071C network analyzer. For pulsed qubit measurements, we use a Quantum Instrument Control Kit based on the Xilinx RFSoC ZCU111 FPGA. Qubit pulses are directly synthesized by the FPGA, while measurement pulses are generated with a heterodyne conversion setup, as shown in Fig. A6. With the spectral layout of each device determined, we select filter networks to minimize unwanted images and harmonics from the FPGA for both the qubit and readout pulses, with a broadband example configuration shown in Fig. A6. The FPGA and carrier signal generator are clocked
to a 10 MHz rubidium source for frequency stability.

Appendix G: Material Loss Probed by Resonator Quality Factor

![Graphs](image)

**FIG. A7.** (a) Power dependence of the internal quality factor for a readout resonator ($Q_i = 2.6 \times 10^5$) with no qubit present. The red line is a fit to a model including loss from two-level systems (TLS). The insets show the lineshape and fits at an average photon occupation $\bar{n}_{ph} \approx 0.96$. (b) Internal quality factor of resonators without qubits measured as a function of temperature. Solid lines are fits to a model including TLS loss and quasiparticle loss. The three red resonators are formed from the wiring layer, and the blue resonators from the base electrode. Measurements are taken at $\bar{n}_{ph} \approx 10^5$ so some TLS loss is saturated. (c) Qubit quality factors $Q_i$ plotted as a function of their readout resonator quality factors $Q_i$ (measured at $n_{ph} < 1$). A grey line indicates a 1:1 relationship.

To compare qubit loss contributions from material sources with contributions from the junction itself, we measure quality factors for readout resonators subject to the same fabrication conditions, but with no qubits attached. A typical normalized transmission spectrum of a resonator taken at a low average photon number ($\bar{n}_{ph} \approx 0.96$) is shown in the inset of Fig. A7a. On resonance, we observe a dip in magnitude, which at low powers is described well by [62]:

$$S_{21} = 1 - \frac{Q}{Q_c} \frac{e^{i\phi}}{1 + 2iQ \frac{\bar{n}_{ph}}{\omega_0}}$$

where $Q^{-1} = Q_i^{-1} + \text{Re}[Q_c^{-1}]$ and the coupling quality factor $Q_c = Q_e^{-1} e^{-i\phi}$ has undergone a complex rotation due to minor impedance mismatches. We plot fitted internal quality factors in Fig. A7a, finding that $Q_i$ increases with power. This behavior is entirely captured by a power dependent saturation mechanism [63], suggesting the dominant loss mechanism in the resonators arises from coupling to two-level systems.

We further investigate limits on the resonator loss by using increased temperatures to further saturate the two-level systems. In Fig. A7b we plot $Q_i$ measured at $\bar{n}_{ph} \approx 10^4$ as a function of temperature (grouped by fabrication layer), with solid lines corresponding to a model of the form

$$Q_i(T)^{-1} = Q_{\text{other}}^{-1} + Q_{\text{TLS}}(T)^{-1} + Q_\sigma(T)^{-1}$$

where $Q_{\text{TLS}}$ is the saturating loss mechanism from two-level systems [63], $Q_{\text{other}}$ is a temperature independent upper bound arising from other sources of loss, and the conduction loss $Q_\sigma$ is given by [54]:

$$Q_\sigma(T) = \frac{1}{\alpha} \frac{\sigma_2(T, T_c)}{\sigma_1(T, T_c)}$$

where $\sigma_1$ and $\sigma_2$ are the real and imaginary parts respectively of the complex surface impedance, calculated by numerically integrating the Mattis-Bardeen equations for $\sigma_1/\sigma_n$ and $\sigma_2/\sigma_n$ [54]. $T_c$ is constrained to the values measured in Appendix B, and $\alpha$ is used as a fit parameter.

Comparing resonators formed during different steps in the fabrication process, we observe that resonators made from the wiring layer exhibit consistently higher quality factors, while resonators from the base layer are lossier and much more variable. Since the sides of the base layer have been exposed to more fabrication steps than the wiring layer, the surface niobium of this layer has a much longer chance to oxidize, and has the additional potential to host
lossy dielectrics from un-removed spacer material. Thus, while we have improved losses in the wiring layer to about 
\( Q_{TLS} \sim 0.9 \times 10^6 \) by reducing fluorocarbon formation, our devices are still loss-limited to approximately \( 2 \times 10^5 \) by
two-level systems in the surfaces of the base electrode.

To investigate the relationship between qubit and readout resonator decoherence, we also measure quality factors of the readout resonator for each qubit. At single-photon powers, the readout resonator is maximally susceptible to material-based loss from two-level systems in its surface, but due to the hybridization of its electric field with the qubit mode will also interact with the materials in the qubit. In Fig. A7, we compare qubit quality factors \( Q_1 \) with the single-photon readout quality factor \( Q_i \) for each of the devices from Fig. 3. On average, we observe that the two quality factors are close to a one to one relationship (as indicated by the grey line), with device variations within a factor of 3 or so. While a direct correlation between the two cannot be extracted from this data, this is to be expected for loss dominated by inhomogeneous material defect distributions between the resonator and qubit. Nevertheless, the similarity of the two quality factors leads us to conclude the qubit and resonator are likely limited by similar decoherence mechanisms.