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ABSTRACT

A challenge faced by experimenters exploring hybrid quantum systems is how to integrate and interconnect different materials and different substrates in a quantum-coherent fashion. Here, we present a simple and inexpensive flip-chip bonding process, suitable for integrating hybrid quantum devices on chips from different substrates. The process only requires equipment and materials used routinely for contact photolithography, and it is possible to undo the bonding and reuse the chips. The technique requires minimal compressive force, so it is compatible with a wide range of different substrates. Unlike indium-based bonding, this process does not establish a galvanic connection between the two chips, but as we show, in some situations this is not necessary. We demonstrate the technique using lithographically patterned quarter-wave coplanar waveguide resonators, fabricated on one chip, and couple these inductively to a transmission line patterned lithographically on a separate chip. The two chips have a vertical interchip gap of about 7 μm, and we can repeatedly achieve lateral alignments of better than 2 μm. We measure electromagnetic resonances with low-power ($\sim$1 photon) internal quality factors Q_i around 5×10^5, comparable to single-chip performances, with as-designed coupling quality factors Q_c ranging from 2×10^2 to 5×10^5.

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Hybrid quantum systems, integration of systems with distinct performance advantages, such as high-fidelity gates in one system combined with long coherence times in another, represent a flexible approach to solving a range of scientific and practical problems.[1–8] However, it is technically challenging to integrate devices involving incompatible materials or fabrication processes. One approach, borrowed from the semiconductor industry, is flip-chip integration, where two separate chips are joined face-to-face.[9,10] Recently, efforts to scale up superconducting quantum circuits have involved flip-chip integration with indium bump-bonds, where the indium establishes a superconducting galvanic connection between the two chips.[11,12] While promising, this approach involves multiple metallization steps with challenging surface treatments, requires significant compressive force to establish good bonding, and requires expensive, specialized bonding equipment.

Here, we present an alternative, simple, and highly accessible method for flip-chip integration. Instead of galvanic connections with metal bumps, we bond the substrates using dried photoresist, allowing reuse of the chips by releasing in a solvent such as acetone. The chip-to-chip vertical spacing is set using lithographically patterned epoxy spacers, whose thickness can range from 1 μm to 100 μm, determined by the available cured epoxy thicknesses. After applying a small amount of photoresist to one chip, we align the chips in a standard contact mask aligner, bring them into contact, and allow the photoresist to dry. This involves just one lithographic process and uses no bonding-specific equipment. This method does not establish a galvanic connection between the chips, so care must be taken to avoid extraneous microwave resonances. The two chips communicate across the vacuum gap, for example, with inductive or capacitive coupling, as described below.

Superconducting circuits are very sensitive to material loss,[13–16] and the photoresist and photodefined-epoxy used here could be problematic. We test this by bonding superconducting coplanar waveguide resonators on one chip to a transmission line probe on the second

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chip, providing a proxy for qubit measurements.[17,18] We use a standard "hanger" measurement configuration where we couple a transmission line to several parallel coplanar waveguide resonators, with resonators and transmission line on separate chips. The resonators and transmission line are patterned on sapphire substrates, but this technique works with a wide variety of materials. In Ref. 7, a superconducting qubit on sapphire is coupled to a surface acoustic wave resonator patterned on lithium niobate.

As there is no galvanic connection between the chips, they interact through free-space coupled electromagnetic fields. Two methods to create the coupling are via an interchip capacitance or a mutual inductance. Inductive coupling has a weaker dependence on the interchip vertical spacing d and can be established separately from the strong capacitive coupling between the ground planes of the two chips. Inductive coupling is also compatible with superconducting coupling strategies involving tunable Josephson inductances.[7,19] In Fig. 1, we illustrate the method used here: inductive coupling between circuits on separate chips using short lengths of coplanar waveguide on each chip, aligned parallel to one another. Each coplanar waveguide is shorted to its ground plane, shown in Fig. 1(a). Each coplanar waveguide segment acts as an inductor L and shares a mutual inductance M, as drawn in Fig. 1(b).

We simulate this geometry with finite element software (Sonnet Software, Syracuse, NY), extracting the inductances L and M from the impedance matrix Z.[20] The ratio M/L, which is at most unity, is a useful measure of the coupling between the chips. In Fig. 1(c), we plot the simulated inductive coupling ratio M/L vs interchip distance d, for different ground-to-center strip spacings s. The ratio M/L scales much more favorably with distance d, decreasing by only about a factor of two as we change d from 2 μm to 20 μm. This weak dependence makes it easier to achieve strong and predictable interactions with larger ($\sim$10 μm) interchip distances and makes the design robust to fabrication and assembly variations. For comparison, we plot the $1/d$ dependence of a parallel-plate capacitor, which decreases an order of magnitude when we change d from 2 μm to 20 μm. In Fig. 1(d), we show the effect of lateral misalignment Δy. The design is robust to lateral misalignment up to about $\Delta y \approx 10\,\mu$m, which is straightforward to achieve. We expect alignment errors along y to be dominant. Misalignment along x, parallel to the waveguides, simply changes the overlap length ℓ, which is roughly proportional to M. The primary effect of small in-plane rotation errors is local translations Δx and Δy,

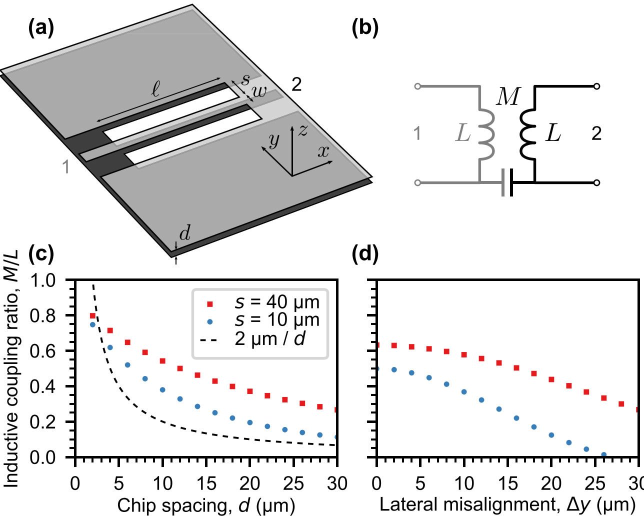

FIG. 1. Inductive coupling scheme and simulations. (a) Schematic of two shorted coplanar waveguide segments, one on each chip. Each forms an inductor L, with a shared mutual inductance M due to the overlap length ℓ. The coplanar waveguide has center trace width $w = 20\,\mu$m and center-to-ground spacing $s = 40\,\mu$m; the two chips are separated by distance d. The two microwave ports are labeled 1 and 2. (b) Circuit diagram for (a). Note the capacitance between the ground planes of the two chips. (c) Finite element simulation results for the inductive coupling ratio M/L as a function of interchip spacing d. Simulations are for $s = 40\,\mu$m [as pictured in (a)] and $s = 10\,\mu$m, which gives a $\approx 50\,\Omega$ transmission line. We plot for comparison (2 μm)/d to exhibit the $1/d$ dependence of a parallel plate capacitance; this falls off much more quickly with d than the mutual inductance. (d) Additional simulation results, M/L vs lateral misalignment Δy, for two values of s, with $d = 6.5\,\mu$m.

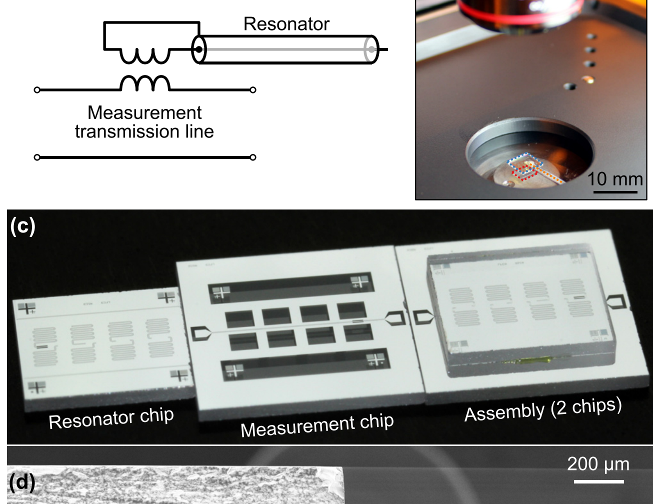

FIG. 2. Flip-chip assembly. (a) Circuit diagram for a coplanar waveguide resonator inductively coupled to a measurement coplanar waveguide on a separate chip. The shorted end of the quarter-wave resonator is placed above the measurement transmission line, creating a mutual inductance between the transmission line and resonator. (b) Photograph of the contact aligner during the assembly process. The two chips are outlined in blue (6 mm measurement chip) and red (4 mm resonator chip with epoxy spacers and glue). We use a machined acrylic plate to transfer the mask vacuum to the 6 mm chip, which is held face-down beneath the plate. The hole that transfers the vacuum is indicated with an orange line. (c) Photograph showing the flip-chip assembly. Right: Complete flip-chip assembly, which is made of a 4 mm chip with resonators inverted and attached to a 6 mm chip with a measurement transmission line. A small amount of glue is visible along the lower edge of the 4 mm chip. Center: A separate 6 mm chip with a measurement transmission line. Left: A separate 4 mm chip with resonators and epoxy spacers. (d) Scanning electron micrograph of assembled chips, with an estimated spacing of 7 μm. A small amount of photoresist can be seen on the right side, at the join between the two chips.

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while small chip tilts cause local spacing differences. We note that these calculations do not account for kinetic inductance, which would increase L without affecting M; this can be significant in some materials such as titanium nitride.[21–24]

We employ the inductive coupling scheme to couple a quarter-wave coplanar waveguide resonator to a measurement coplanar waveguide on a separate chip. This is shown in Fig. 2(a). This circuit is complementary to the usual capacitive hanger measurement.[14] Here, the measurement waveguide is under the short-circuit side of the quarter-wave resonator, where the current is maximized. The mutual inductance M allows energy to enter and leave the resonator through the measurement waveguide, quantified by the coupling quality factor

$$Q_c = \frac{1}{8\pi}\left(\frac{Z_0}{f_0 M}\right)^2, \quad (1)$$

where f_0 is the resonance frequency and $Z_0 \approx 50\ \Omega$ is the characteristic impedance of the coplanar waveguide. Following a calculation analogous to Ref. 14, we determine the normalized microwave transmission $\tilde{S}_{21}$ through the measurement waveguide

$$\frac{1}{\tilde{S}_{21}} \approx 1 + e^{i\phi}\frac{Q_i}{Q_c}\frac{1}{1 + i2Q_i\delta x}, \quad (2)$$

where Q_i is the internal quality factor of the resonator, $\delta x = (f - f_0)/f_0$ is the relative frequency shift from resonance, and $e^{i\phi}$ a phase factor accounting for a small series impedance mismatch $\Delta Z \ll Z_0$.

The inductive coupling geometry described in Fig. 1 can be varied quite a bit, with a range of about two orders of magnitude in M, or four orders of magnitude in coupling strength Q_c. We test this by building eight coplanar waveguide resonators, each with a slightly different length (hence resonance frequency) and a different Q_c. The coupler designs are listed in Table I. The mutual inductance is proportional to the coupler length ℓ_c. For resonator 1, we minimize Q_c (increasing the coupling) by using wider ground plane spacing $s_c = 40\ \mu$m in the coupler, while for resonators 2 to 4, we gradually increase Q_c by decreasing the coupler length ℓ_c, and for resonators 5 to 8, we further increase Q_c by introducing an intentional lateral misalignment Δy between the coupler and the measurement waveguide.

The flip-chip assembly process is illustrated in Fig. 2. We evaporate 100 nm of aluminum on a double-side polished sapphire wafer and pattern by plasma-etching the aluminum. We pattern epoxy spacers (SU-8 3005 photoresist, 7 μm thick) prior to dicing the wafer. The epoxy spacers are only needed on one of the chips.

We bond the two chips together in a standard manual mask aligner (Karl Suss MJB4), shown in Fig. 2(b). We use the mask vacuum to suspend one chip upside-down and fix it in place; it is important that it is double-side polished and transparent for alignment. The second chip has the resonators and epoxy spacers, the latter designed to contain the photoresist (nLOF 2070) "glue." We did observe that after two thermal cycles to cryogenic temperatures, the photoresist becomes quite brittle. We chose nLOF 2070 based on room-temperature mechanical tests, and there may be more robust, lower-loss alternatives. We apply the photoresist manually, covering roughly 2 mm along the two opposite edges of the chip. We align the chips, bring them into contact, and solidify the photoresist by heating gently with a hot air gun for about 10 min. A completed assembly is shown in Figs. 2(c) and Fig. 2(d). The two chips are separated by about 7 μm, with a typical tilt of about 0.03°. Typical lateral alignment error is less than 2 μm in translation and 0.03° in rotation, well within the tolerances suggested by the simulations in Fig. 1.

We characterize the device by cooling it in a dilution refrigerator (base temperature 7 mK) and measuring its microwave transmission S_{21}. The device is wirebonded in an aluminum sample box with multi-stage magnetic shielding, the input line is heavily attenuated and filtered, and the output line includes a high electron mobility transistor amplifier at 4 K (Low Noise Factory) as well as room temperature amplifiers (Miteq AFS3). Representative measurements are shown in Fig. 3, showing the eight desired coplanar waveguide resonances. There is an additional unidentified resonance near 4.5 GHz, which may be a slotline or other unwanted mode. In Fig. 3(b), we show the detailed response for the highest Q_c resonance, with magnitude normalized to approach 0 dB off-resonance, and we subtract a linear offset from the phase. Following Ref. 14, a fit to Eq. (2) allows us to extract f_0, Q_i, Q_c, and the mean photon number n. Similar measurements were made on the other resonances.

In Fig. 4, we summarize the fit quality factors. Figure 4(a) compares the measured coupling quality factors Q_c to their design values, discussed above. We achieve the desired range of more than three orders of magnitude in Q_c, illustrating this technique's flexibility. The measured

TABLE I. Coupler designs for the eight coplanar waveguide resonators. The ground-center conductor spacing is s_c and the coupler length ℓ_c; Δy is the intentional lateral misalignment (see Fig. 1). The measured resonance frequencies f_0 are within 10% of the design frequencies, and the frequency spacings are as designed for resonances 3–8 (the two lowest-Q_c resonators were offset differently, perhaps due to their longer couplers). Outside the coupler region, the resonators and measurement transmission line are all coplanar waveguides with $w = 20\ \mu$m and $s = 10\ \mu$m, giving $Z_0 \approx 50\ \Omega$. The design coupling quality factors Q_c are based on the simulations in Fig. 1, with interchip distance $d = 6.5\ \mu$m. We also include the measured values for f_0 and Q_c fit from experimental data.

	s_c (μm)	ℓ_c (μm)	Δy (μm)	Design f_0 (GHz)	Measured f_0 (GHz)	Design Q_c	Measured Q_c
1	40	300	0	5.25	5.676	2.3×10^2	1.55×10^2
2	10	300	0	5.37	5.880	6.9×10^2	5.31×10^2
3	10	100	0	5.49	5.798	6.0×10^3	4.73×10^3
4	10	40	0	5.93	6.196	3.2×10^4	1.07×10^4
5	10	40	5	5.85	6.121	4.5×10^4	1.15×10^4
6	10	40	10	5.76	6.033	6.3×10^4	3.25×10^4
7	10	40	15	5.67	5.949	1.5×10^5	1.23×10^5
8	10	40	20	5.59	5.862	5.9×10^5	4.44×10^5

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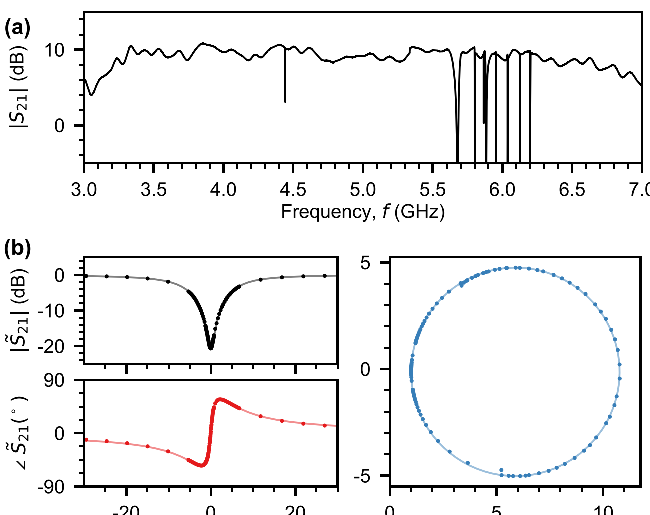

FIG. 3. Microwave transmission measurements. (a) Raw transmission magnitude $|S_{21}|$ through the measurement transmission line. The overall level is arbitrary, dictated by attenuation and amplification in the signal path. There are eight coplanar waveguide resonances (5.6 GHz to 6.2 GHz) and an additional unidentified resonance at 4.5 GHz. This spurious resonance has $Q_i \approx 6 \times 10^4$ (much lower than the coplanar waveguide resonances) and $Q_c \approx 5 \times 10^4$. The frequency spacing of this scan is 31.25 kHz. (b) Normalized transmission $\tilde{S}_{21}$ close to the highest-Q_c coplanar waveguide resonance. The magnitude $|\tilde{S}_{21}|$ (black) and phase $\angle\tilde{S}_{21}$ (red) are plotted vs frequency detuning $f - f_0$, where the resonator frequency is $f_0 = 5.862$ GHz. The inverse $1/\tilde{S}_{21}$ (blue) is plotted in the complex plane (horizontal axis: real part, vertical axis: imaginary part). This measurement is at relatively high power, with $n = 4.0 \times 10^6$ photons in the resonator. Solid lines are fits to Eq. (2).

Q_c values are systematically lower than the design values; the simulations were two-port simulations as in Fig. 1, and more comprehensive simulation geometries may yield better results. Significantly, the effects of coupler spacing s_c, length ℓ_c, and lateral offset Δy are all consistent with the simulations. This also suggests that the chip alignment and spacing did not change significantly when the sample was cooled to cryogenic temperatures. Figure 4(b) shows the measured internal quality factor Q_i vs the mean photon number n, which is proportional to the drive power. We perform power-dependent measurements on the three highest-Q_c resonances as the measurement time is much faster when $Q_c \sim Q_i$. We observe the characteristic sigmoidal behavior, where Q_i decreases with n, reaching a plateau at the small $n \sim 1$ limit, with $Q_i \approx 5 \times 10^5$. This is about an order of magnitude lower than the high power ($n > 10^6$) measurements, and it is consistent with similar single-chip resonator measurements.[14]

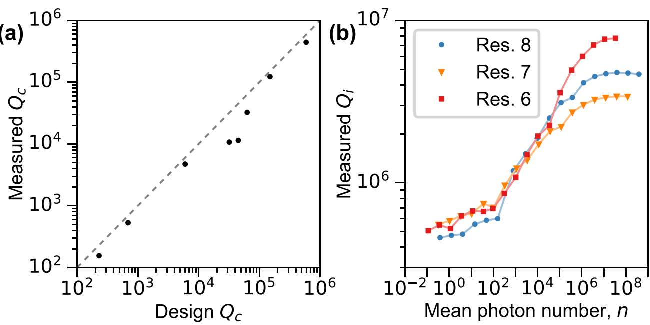

FIG. 4. Quality factor measurements. (a) Measured coupling quality factor Q_c vs the design value. The dashed line represents the ideal case. Uncertainty in each fitted Q_c value is about 2%. (b) Measured internal quality factor Q_i vs the mean photon number n for the three highest-Q_c resonances. Uncertainty in each fitted Q_i value is about 10%. Lines connect the measured data points.

In conclusion, we have demonstrated a simple method for flip-chip integration using only basic photolithography equipment. The inductive coupling scheme we use here is robust to errors in interchip distance and alignment, and it allows designs with a wide range of coupling strengths. This technique is compatible with low-loss superconducting circuits, opening up a wide range of experiments integrating hybrid quantum systems, as devices with incompatible materials can be fabricated separately before being assembled together. A specific example is described in Ref. 7.

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